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Topics on Compilers

Introduction to CGRA

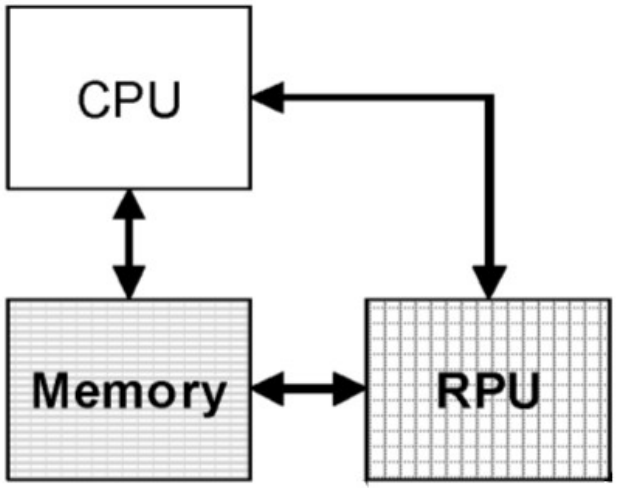
Spring 2011

Introduction to CGRA

- **Reconfigurable Architectures**
  - reconfigurable hardware (*reconfigware*)
    - implement specific hardware structures dynamically and on-demand
    - high performance at low power
      - outperform general purpose processors in many applications by providing spacial, parallel and specialized computation
      - very interesting for mobile & embedded systems
    - typical organization
      - logic blocks in a 2-D array
      - routing resources

Introduction to CGRA

- **Reconfigurable Architectures**
  - reconfigurable hardware (*reconfigware*)
    - best known reconfigurable architectures: FPGAs
      - configuration block: bit-level
      - data routing the major challenge
      - reconfiguration is slow
      - automatic mapping of sequential C programs very difficult
    - usually part of a SoC design



(image source: Compiling for Reconfigurable Computing: A Survey, CSUR)

Introduction to CGRA

- **Reconfigurable Architectures**
  - fine-grained vs. coarse-grained reconfigurable architectures
    - fine-grained
      - programmable blocks and routing resources at the bit-level
      - can build “anything”
        - 12-bit fixed-point arithmetic for a signal-processing app
        - 14-bit butterfly routing network for a FFT
    - coarse-grained reconfigurable architectures (CGRA)
      - sometimes also referred to as “coarse-grained reconfigurable array”
      - programmable blocks and routing resources > 1 bit, e.g., 32 bit
      - less flexible than fine-grained reconfigurable architectures
      - but
        - easier to program
        - fast reconfiguration

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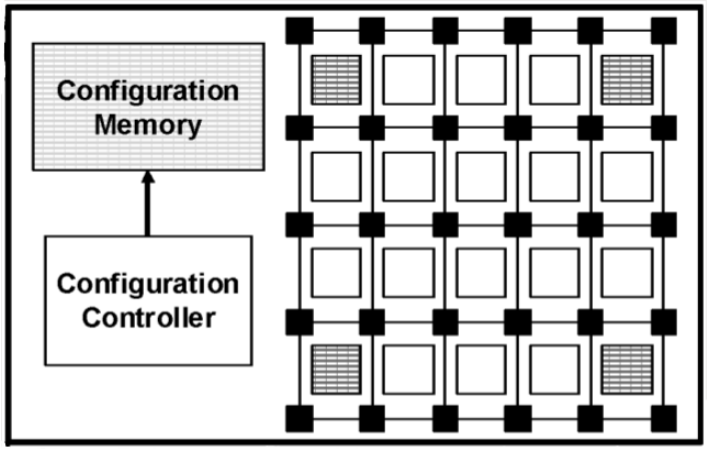
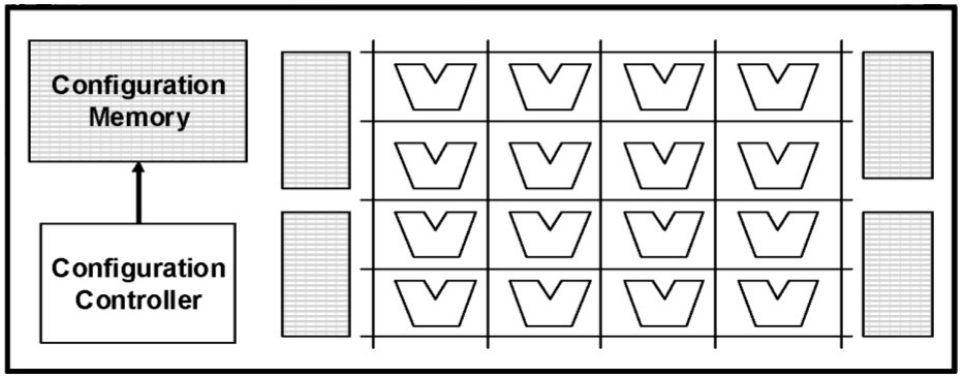
- **Reconfigurable Architectures**
  - fine-grained vs. coarse-grained reconfigurable architectures
    - fine-grained



    - coarse-grained reconfigurable architectures (CGRA)



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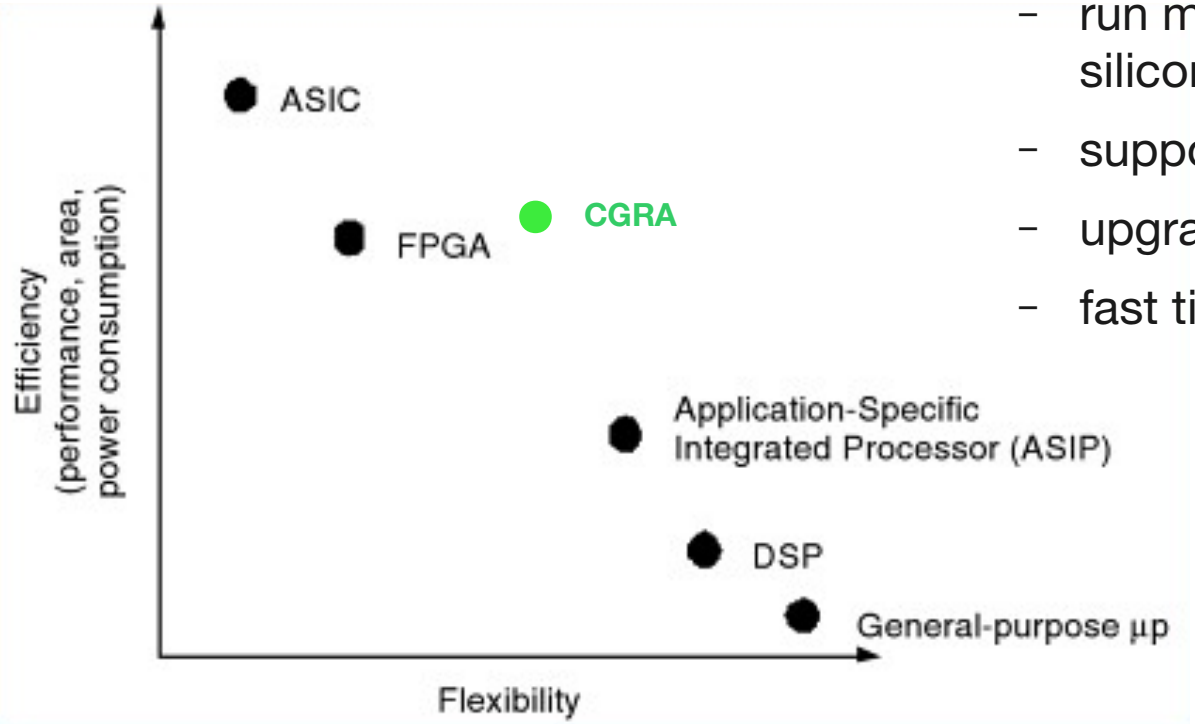
- **Coarse-grained reconfigurable architectures**



(source: Fine- and Coarse-Grain Reconfigurable Computing, Springer)

- programmability and flexibility
  - run multiple kernels on the same silicon die
  - support several standards
  - upgradability
  - fast time-to-market

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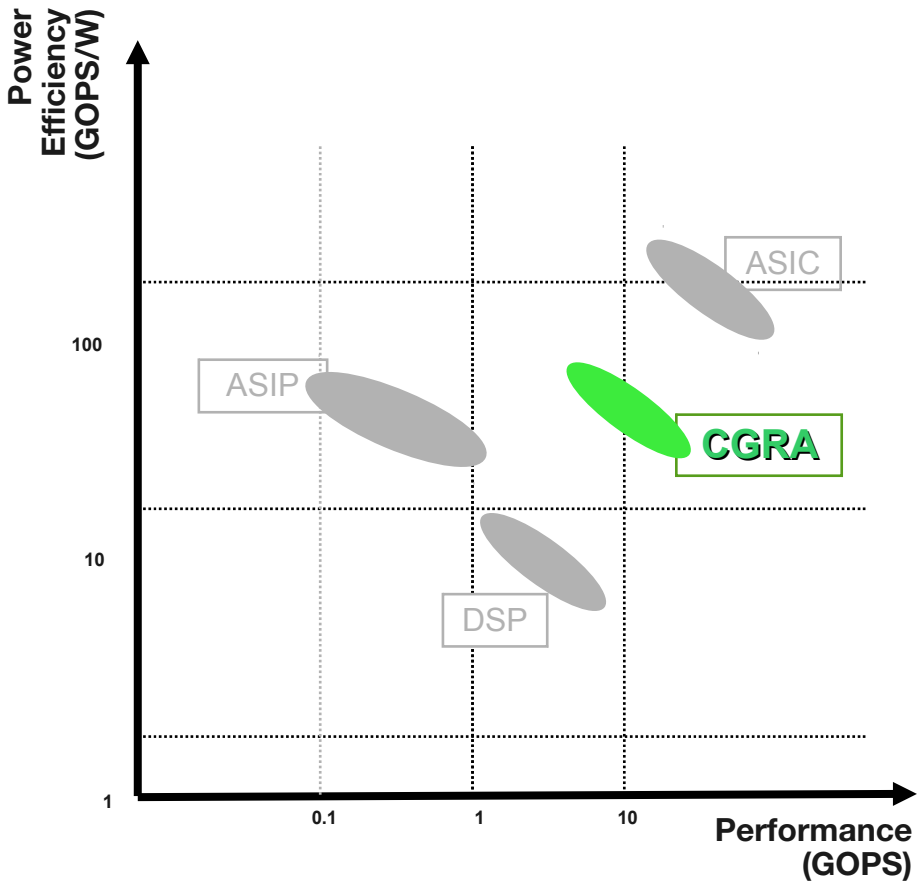
- **Coarse-grained reconfigurable architectures**



- efficiency
  - low power consumption
  - high performance

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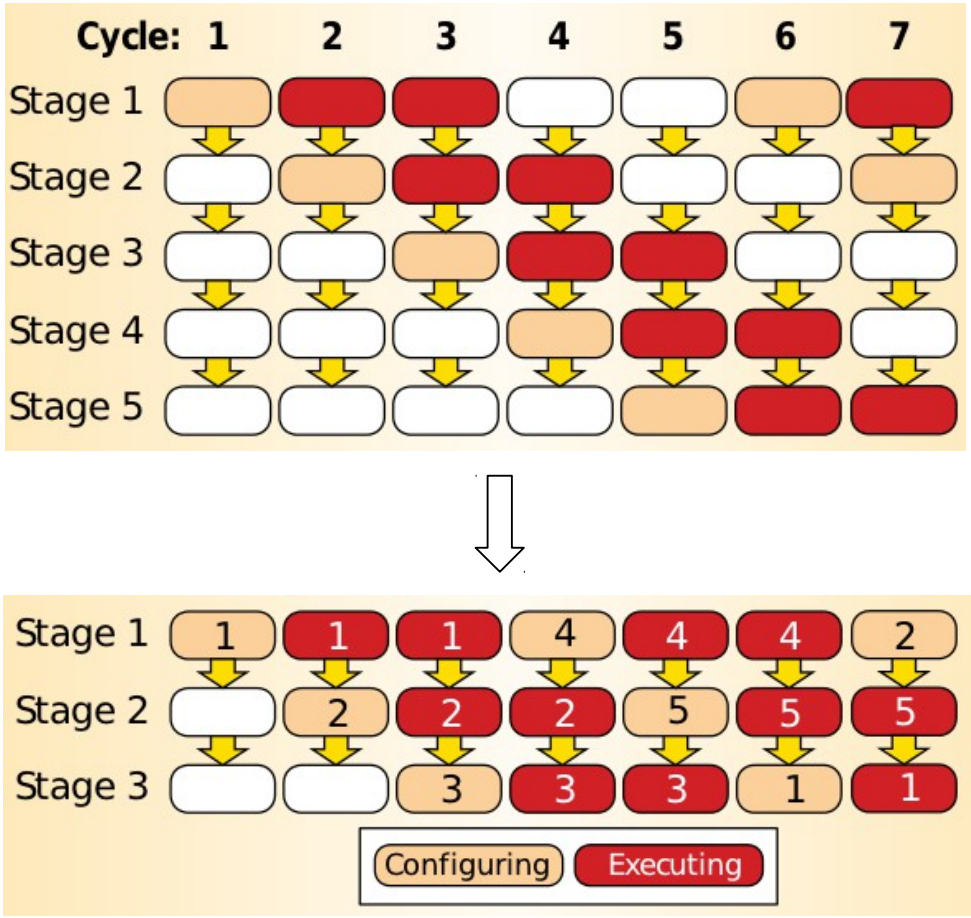
- **Coarse-grained reconfigurable architectures**
  - PipeRench (Goldstein et al., 1999)
    - naturally map application stages to a pipelined reconfigurable architecture



(image source: PipeRench: A Reconfigurable Architecture and Computer, IEEE)

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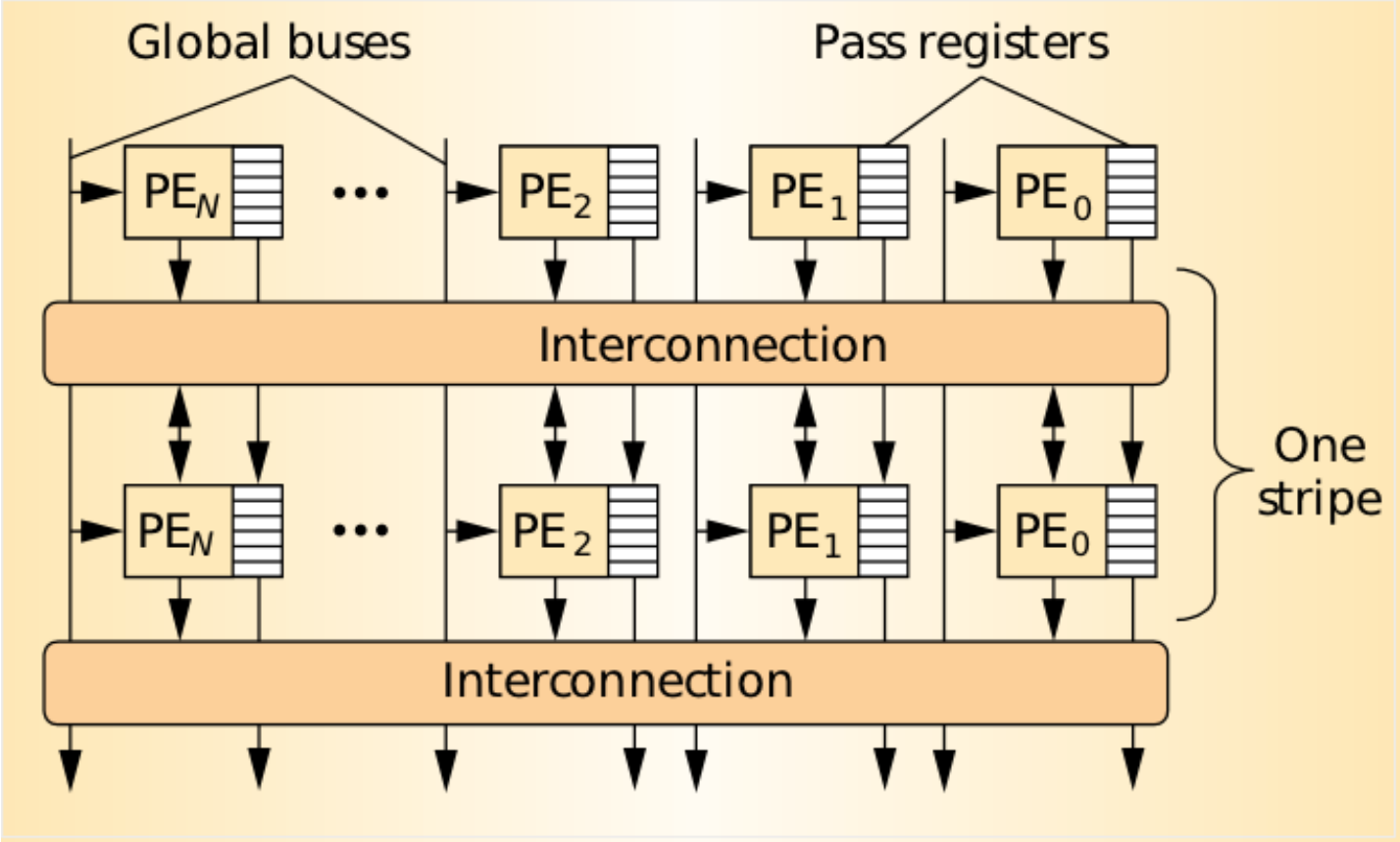
- **Coarse-grained reconfigurable architectures**
  - PipeRench (Goldstein et al., 1999)
    - architecture description flexible
    - source language: dataflow intermediate language



(image source: PipeRench: A Reconfigurable Architecture and Computer, IEEE)

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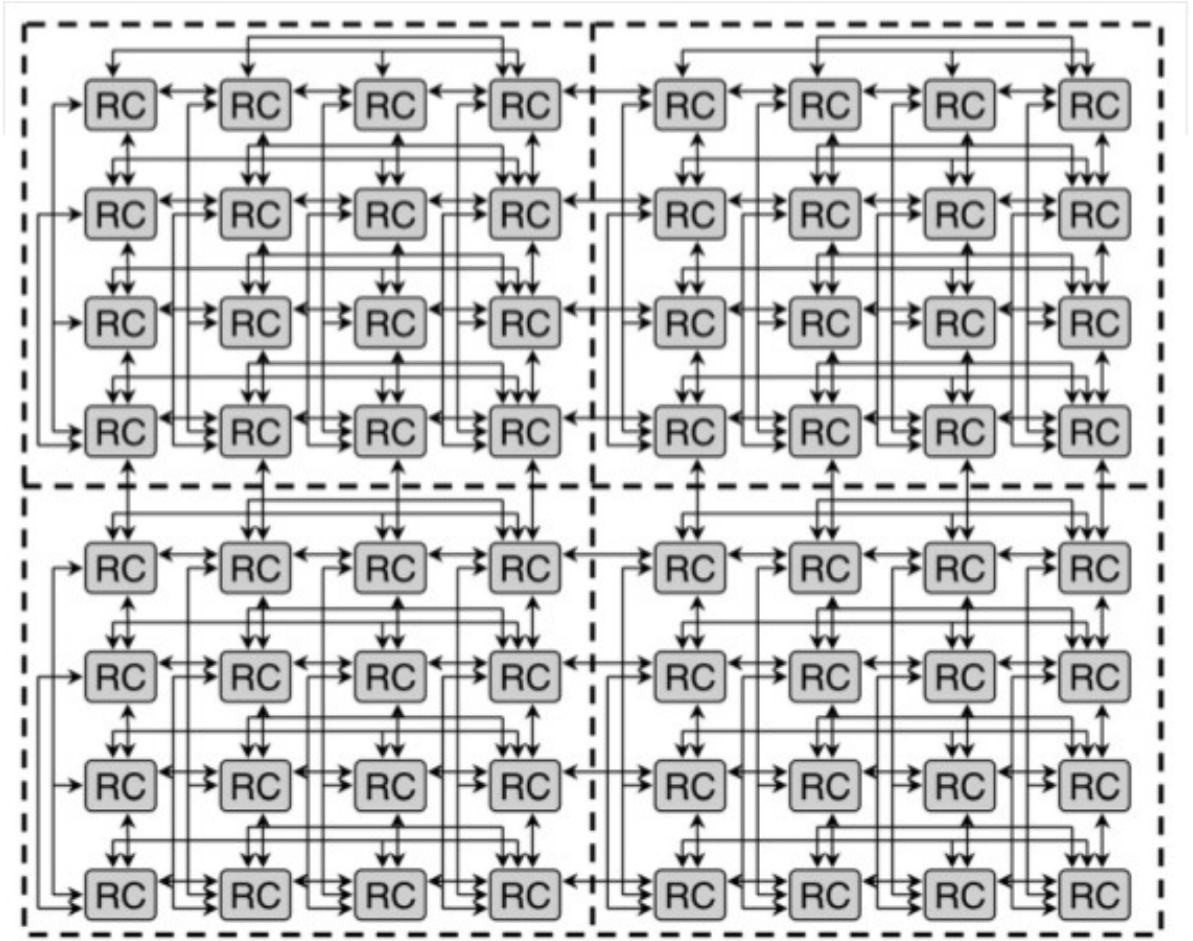
- **Coarse-grained reconfigurable architectures**
  - MorphoSys (Singh et al., 2000)
    - 8/16 bit FU (reconfigurable cell) array



(image source: MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications, IEEE TC)

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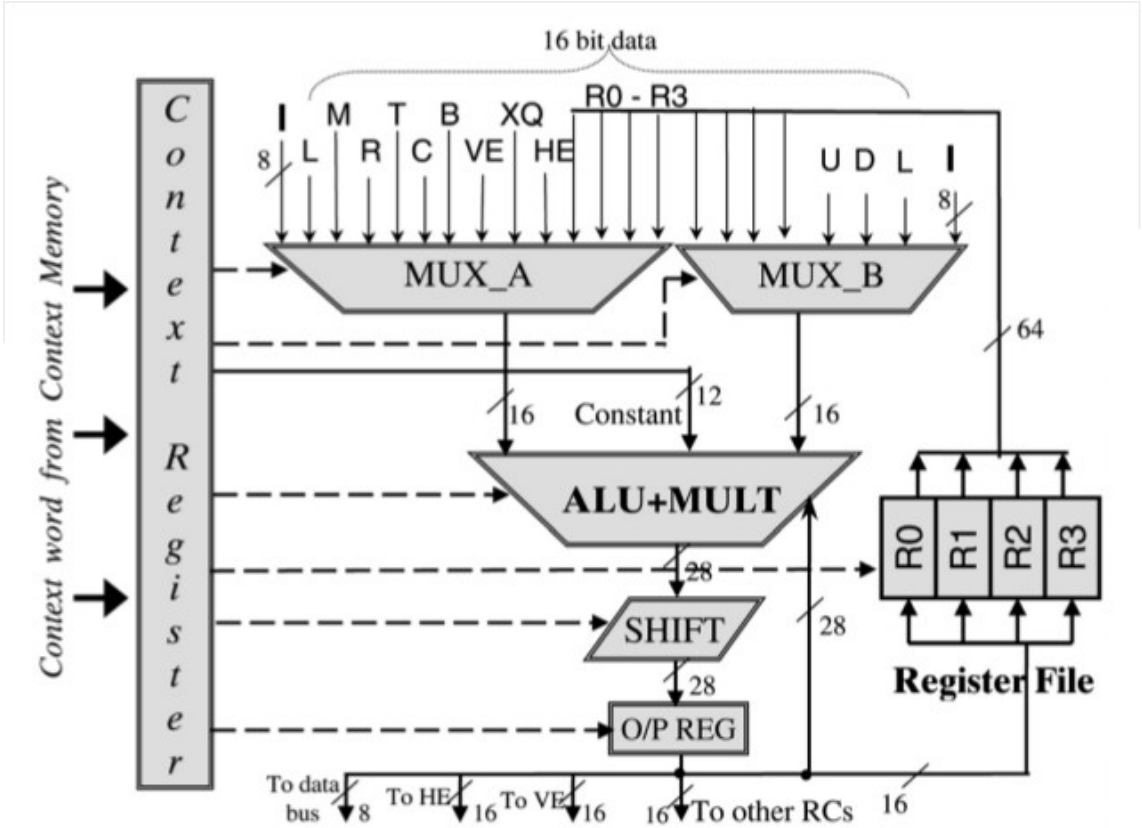
- **Coarse-grained reconfigurable architectures**
  - MorphoSys (Singh et al., 2000)
    - detail view of one RC (reconfigurable cell)



(image source: MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications, IEEE TC)

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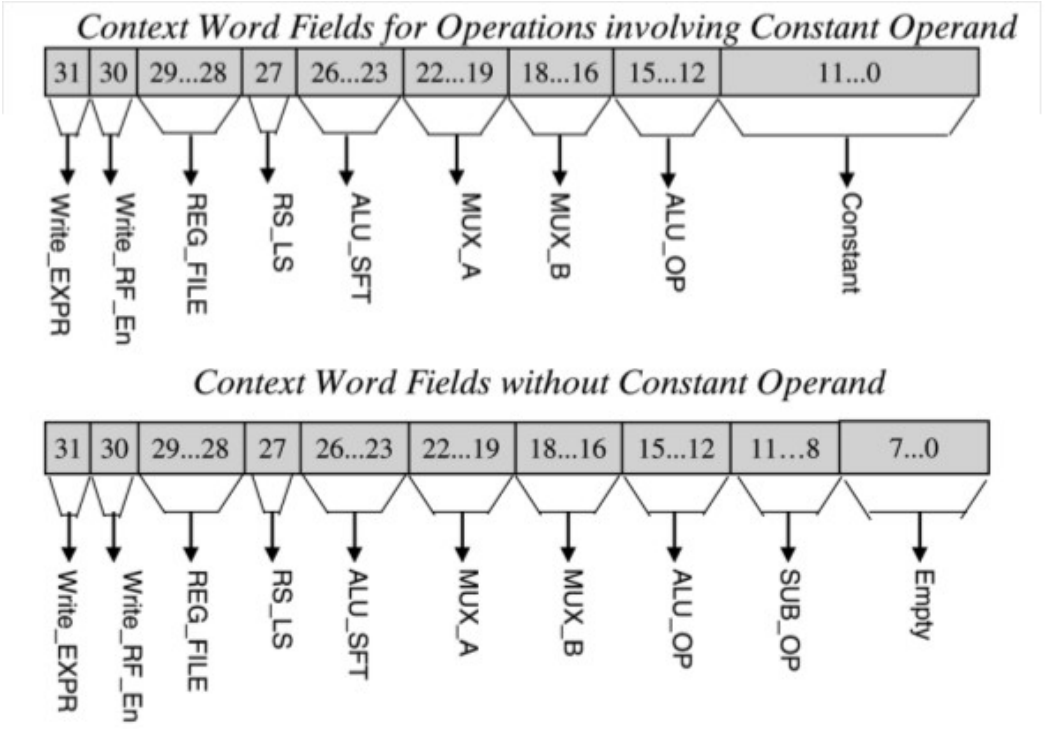
- **Coarse-grained reconfigurable architectures**
  - MorphoSys (Singh et al., 2000)
    - configuration of an RC



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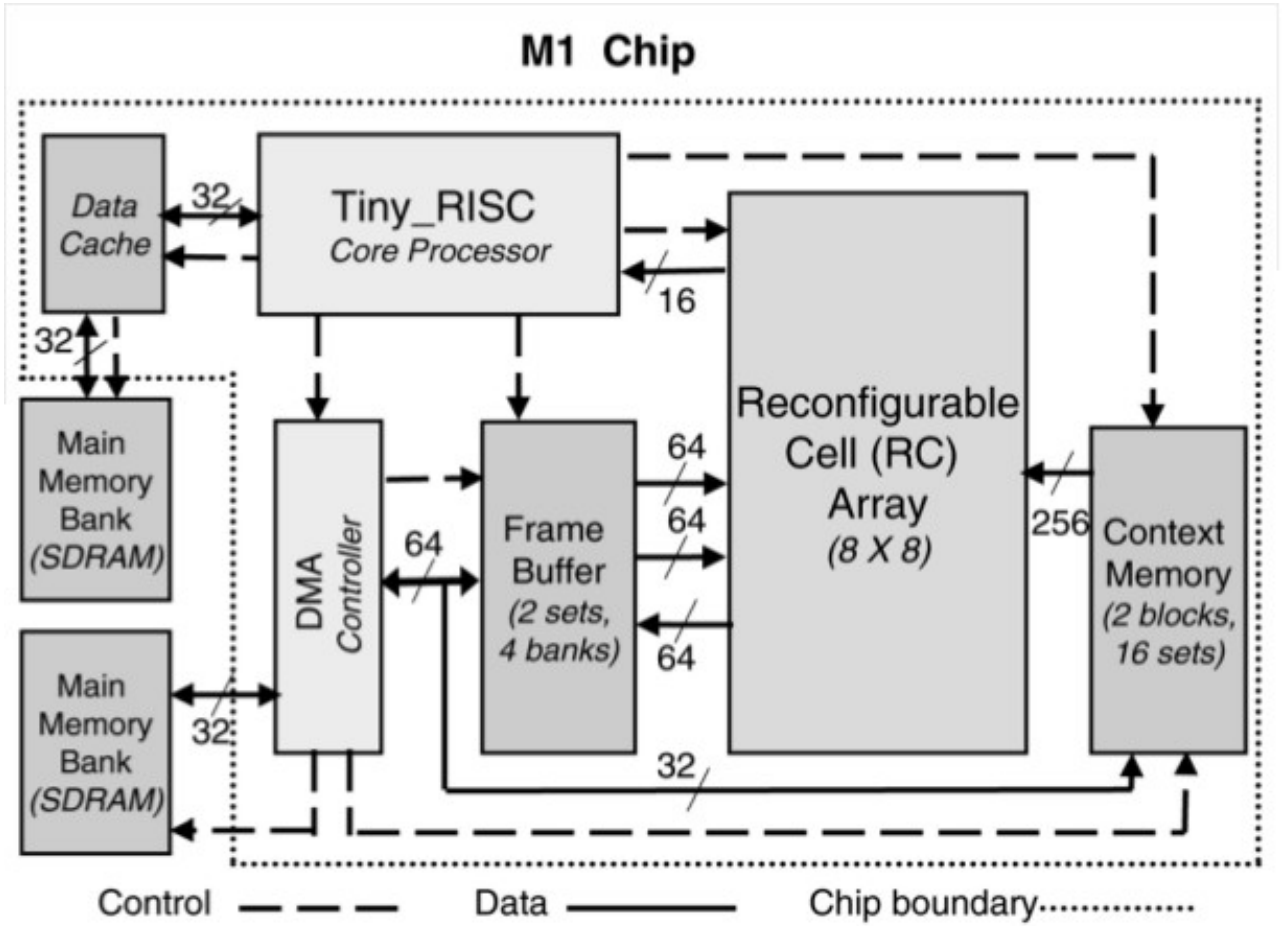
- **Coarse-grained reconfigurable architectures**
  - MorphoSys (Singh et al., 2000)
    - system integration



(image source: MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications, IEEE TC)

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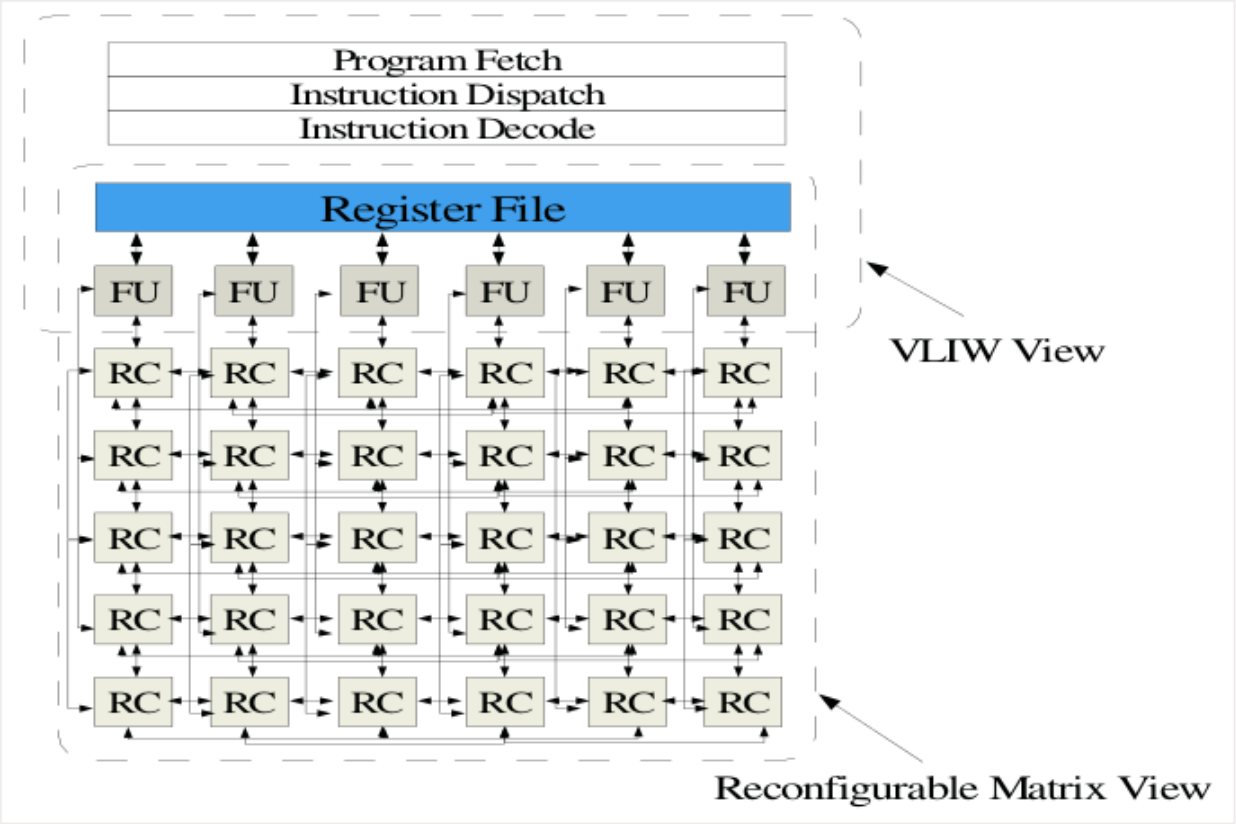
- **Coarse-grained reconfigurable architectures**
  - ADRES (Mei et al., 2003)
    - combined VLIW / CGRA processor



(image source: ADRES: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix, Springer LNCS)

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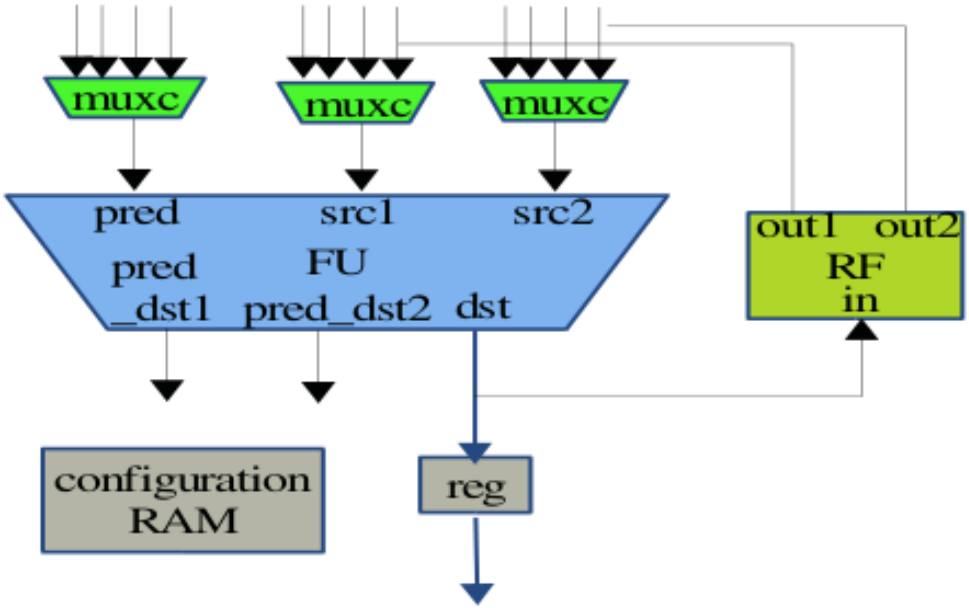
- **Coarse-grained reconfigurable architectures**
  - ADRES (Mei et al., 2003)
    - reconfigurable cell



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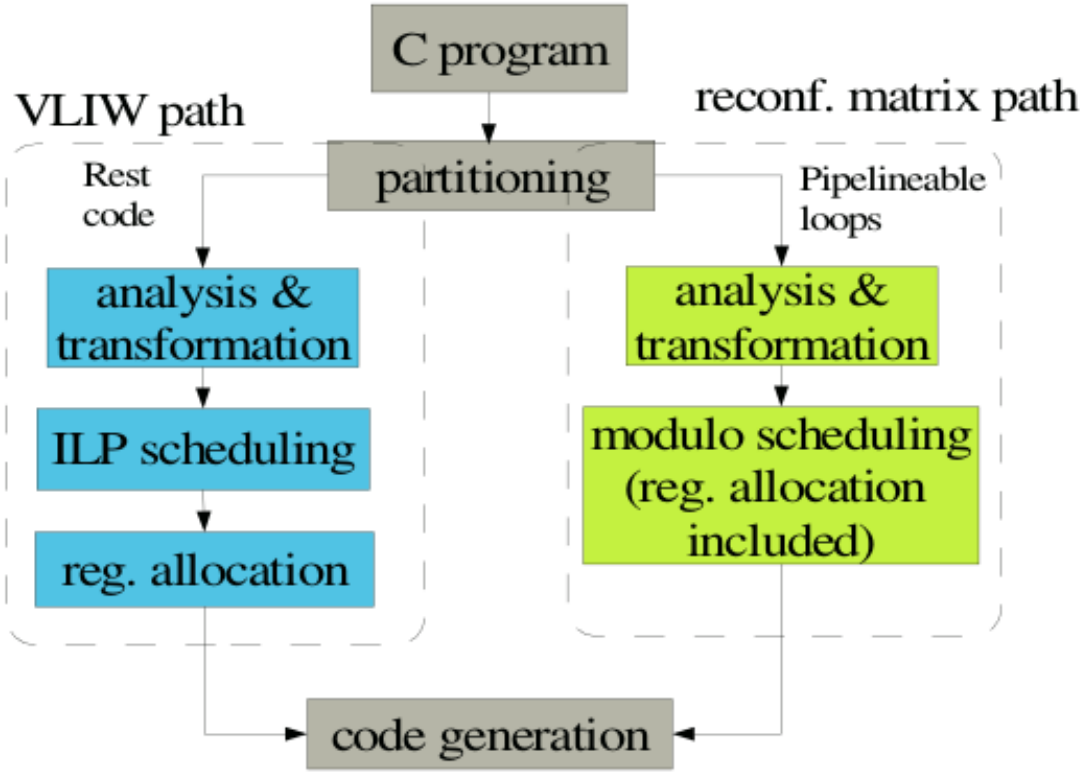
- **Coarse-grained reconfigurable architectures**
  - ADRES (Mei et al., 2003)
    - VLIW/CGA interaction



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Introduction to CGRA

- **Compiling for CGRA**
  - typically no control flow
    - innermost loops
    - if-conversion
  - modulo scheduling
    - software pipelining
    - compute II based on data flow graph
  - placement & routing
    - mapping of the data flow graph to the architecture graph
    - several techniques
      - node-centric: simulated annealing
      - edge-centric

Introduction to CGRA

- Further Reading:
  - Compiling for Reconfigurable Computing: A Survey
    J. Cardoso, P.Diniz, M. Weinhardt, ACM Computing Surveys
  - Piperench: A Reconfigurable Architecture and Computer
    S. Goldstein et al., IEEE Computer
  - MorphoSys: an integrated reconfigurable system for data-parallel and computation-intensive applications
    H. Singh, IEEE Transactions on Computers
  - ADRES: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix
    B. Mei et al., Springer LNCS