Jaejin Lee
(이재진)
Department of Computer Science and Engineering
Seoul National University
Seoul 151-744, Korea
Office Phone: +82-2-880-1863
E-mail: jaejin@snu.ac.kr
Home Page: http://aces.snu.ac.kr/~jlee

EDUCATION

Ph.D. in Computer Science Aug 1995 – Oct 1999
Advisor: David A. Padua
Thesis: Compilation Techniques for Explicitly Parallel Programs
University of Illinois at Urbana-Champaign (UIUC), IL, USA

M.S. in Computer Science Sep 1993 – Jun 1995
Stanford University, CA, USA

B.S. in Physics Mar 1986 – Feb 1991
Seoul National University (SNU), Seoul, South Korea

RESEARCH INTERESTS

Programming systems of heterogeneous machines (GPUs and FPGAs)
Parallelization and optimization of deep learning frameworks
Quantum computing

EXPERIENCES

Director, SW Star Lab., SNU Apr 2018 – Feb 2026
(과학기술정보통신부/정보통신방송연구개발사업/SW 컴퓨팅산업원천기술개발사업/SW 스타랩)
Institute for Information & Communication Technology Promotion (IITP)/Ministry of Science and ICT

Professor (서울대학교 컴퓨터공학부 교수) Oct 2010 – Present
Associate Head of Academic Affairs (서울대학교 컴퓨터공학부 교무부학부장) Sep 2016 – Aug 2018
Associate Professor (서울대학교 컴퓨터공학부 부교수) Oct 2004 – Sep 2010
Assistant Professor (서울대학교 컴퓨터공학부 조교수) Sep 2002 – Sep 2004
Dept. of Computer Science and Engineering, SNU

Associate Director Sep 2018 – Jan 2019
SNU R&DB Foundation (서울대학교 산학협력사업부단장)
SNU Entrepreneurship Center (서울대학교 창업지원부단장)

Managing Director, Institute of Computer Technology, SNU Nov 2013 – Nov 2015, Sep 2016 – Present
(서울대학교 컴퓨터연구소 운영부장)

Director, Platform Technology Division, Big Data Institute, SNU Jul 2014 – Present
(서울대학교 빅데이터연구원 플랫폼기술부 부장)

EXPERIENCES (cont'd)

Consultant, Samsung Electronics, South Korea
System software area, Software Center, Device Solutions division — Oct 2017 – Sep 2018
(삼성전자 DS 부문 소프트웨어센터 System Software 분야 자문교수)
Big Data/Intelligence/Cloud area, Software Center — Mar 2015 – Apr 2016
(삼성전자 소프트웨어센터 Big Data/Intelligence/Cloud 분야 자문교수)

Director, Center for Manycore Programming, SNU — Apr 2009 – Feb 2018
(미래창조과학부/리더연구자지원사업/창의적연구, 매니코어 프로그래밍 연구단 단장)
National Research Foundation of Korea/Ministry of Science, ICT and Future Planning

Visiting Scholar, Dept. of Electrical and Computer Engineering, Purdue University — Sep 2015 – Aug 2016

ICT Subcommittee Chair, Expert Committee on ICT and Convergence Technology — Jan 2015 – Apr 2016
National Science and Technology Council, Korea (국가과학기술심의회 ICT·융합 전문위원회, ICT 소위원회 위원장)

Member, Expert Committee on Advanced Convergence Technology — Apr 2013 – Jan 2015
National Science and Technology Council, Korea (국가과학기술심의회 첨단융합 전문위원회 위원)

Member, National Supercomputing Practices Committee — Nov 2012 – Nov 2014
Ministry of Science, ICT and Planning, Korea (국가초고성능컴퓨팅 실무위원회 위원)

Member, Review Board, Computer Systems area — Jun 2012 – Jun 2014
National Research Foundation of Korea (한국연구재단 컴퓨터시스템 분야 RB)

Professor in Special Affairs (서울대학교 중앙전산원 특임교수) — Aug 2007 – Sep 2008
Director, System Administration Division (서울대학교 중앙전산원 시스템 부장) — Oct 2004 – Aug 2007
University Computer Center, SNU

Assistant Professor (미국 미시간 주립대학교 컴퓨터공학과 조교수) — Jan 2000 – Aug 2002
Dept. of Computer Science and Engineering, Michigan State University

Visiting Lecturer and Postdoctoral Research Associate — Aug 1999 – Dec 1999
Dept. of Computer Science, UIUC

Research Assistant
Polaris group (Supervisor: David A. Padua)
Dept. of Computer Science, UIUC — Jan 1997 – Aug 1999
Center for Supercomputing Research and Development, UIUC — Jan 1996 – Dec 1997
Stanford Temporal Prover project (Supervisor: Zohar Manna)
Dept. of Computer Science, Stanford University — Sep 1994 – Mar 1995

Summer Intern, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA — Jun 1997 – Aug 1997

Teaching Assistant
CS101: Introduction to Programming for Engineers and Scientists — Fall 1995
Dept. of Computer Science, UIUC
CS1U: Introduction to UNIX — Winter 1995
CS161: Design and Analysis of Algorithms — Spring 1995
Dept. of Computer Science, Stanford University

Military Service, Korean Army — Jan 1991 – Jun 1992

HONORS and AWARDS

IEEE Fellow Jan 2019
for contributions to programming systems of heterogeneous machines

The Okawa Foundation Research Grant Mar 2018
The Okawa Foundation for Information and Telecommunications, Japan

Citation Award, Minister of Science, ICT and Future Planning, Korea Dec 2014
(미래창조과학부 장관 표창)

Citation Award, Director of the National Intelligence Service, Korea Dec 2014
(국가정보원장 표창)

100 Future Technologies and Leading Persons Advancing Korean Industry in 2020 Dec 2013
Listed in Exascale Computer Systems in Software area
The National Academy of Engineering of Korea
(한국공학한림원 2020 년 대한민국 산업을 이끌 미래 100 대 기술과 주역, 소프트웨어 분야 Exascale 컴퓨터 시스템)

Teaching Excellence Award 2011, 2012
College of Engineering, SNU
(서울대학교 공과대학 우수교육상)

Research Excellence Award 2009, 2010
College of Engineering, SNU
(서울대학교 공과대학 우수연구상)

NSF CAREER Award May 2003
National Science Foundation, USA
(awarded but withdrawn before finalization due to the movement to SNU)

Best Paper Award
SCOPES '04: The 8th International Workshop on Software and Compilers for Embedded Systems Sep 2004
MTEAC-5: The 5th Workshop on Multithreaded Execution, Architecture, and Compilation Dec 2001

IBM Ph.D. Fellowship Aug 1997 – May 1999

Korea Foundation for Advanced Studies Fellowship Sep 1997 – Aug 1999
(한국고등교육재단 해외유학 장학금)

RESEARCH GRANTS (1.00 USD = 1,111 KRW as of January 2019)

1. CUDA Programming Environment for FPGA Clusters (FPGA 클러스터 용 CUDA 프로그래밍 환경 기술 개발), PI, Ministry of Science and ICT (과학기술정보통신부/정보통신방송연구개발사업/SW 컴퓨팅산업원천기술개발사업/SW 스타랩), 2,400,000,000 KRW, April 2018 – February 2026
2. Developing High-performance Programming Environments and Computing Systems (초고성능 프로그래밍 환경 및 계산 시스템 개발), PI (with Hyeonsang Eom, Sang Lyul Min, Taekyoung Kwon, Jae Wook Lee, Heonyoung Yeom, Sungjoo Yoo), Ministry of Science and ICT (과학기술정보통신부/차세대정보컴퓨팅기술개발/한국연구재단/초고성능컴퓨팅연구단), 5,838,000,000 KRW, November 2016 – December 2020
3. Developing a Deep Learning Framework for SNPU Systems (SNPU 시스템을 위한 딥 러닝 프레임워크 개발), PI, Samsung Electronics, 459,000,000 KRW, November 2017 – October 2020
4. Parallel Processing Techniques to Improve the Processing Speed of NFA (NFA 연산 속도 개선을 위한 병렬 연산처리기술 개발), PI, SK Hynix, 100,000,000 KRW, December 2017 – November 2019
5. OpenCL Framework for FPGA-based Heterogeneous Systems (FPGA 기반 이종 시스템을 위한 OpenCL 프레임워크), PI, The Okawa Foundation for Information and Telecommunications, Japan, 1,000,000 JPY, December 2017 – November 2018
6. Implementation and Application of Crypto Library for FPGAs (FPGA 용 암호 라이브러리 구현 및 활용), PI, Korea Institute of Information Security and Cryptology (한국정보보호학회), 45,000,000 KRW, February 2018 – November 2018
7. Deep Neural Network Inference Acceleration Environment for Smart Office Implementation (지능형 오피스 구현을 위한 인공신경망 추론 가속환경 개발), PI, Hancom Inc. ((주)한글과 컴퓨터), 100,000,000 KRW, September 2017 – August 2018
8. Center for Manycore Programming (매니코어 프로그래밍 연구단), PI, Ministry of Science, ICT and Future Planning (미래창조과학부/창의적연구/한국연구재단), 5,400,000,000 KRW, April 2009 – February 2018
9. Optimization of Crypto Algorithms using OpenCL Frameworks for FPGAs (FPGA 용 OpenCL 을 사용한 암호 알고리즘 최적화 연구), PI, Korea Institute of Information Security and Cryptology (한국정보보호학회), 45,000,000 KRW, February 2017 – November 2017
10. OpenCL-based Performance Acceleration Environment that Supports Various Platforms (다양한 플랫폼을 지원하는 OpenCL 기반 성능 가속 환경 개발), PI, Hancom Inc. ((주)한글과 컴퓨터), 100,000,000 KRW, February 2016 – January 2017
11. Parallelization Techniques of Integrated Data Processing Systems for the Geostationary Ocean Color Imager (해양탑재체 통합자료 처리시스템 작업 병렬화 기법 연구), PI, Ministry of Oceans and Fisheries (해양수산부/해양수산연구개발사업/한국해양과학기술진흥원, 위탁연구), 40,000,000 KRW, January 2016 – December 2016
12. SRP-based CPU Off-loading Techniques (SRP 기반 CPU Off-loading 기술 개발), PI, Samsung Electronics, 40,000,000 KRW, April 2016 – November 2016
13. Many-SC Programming Model (Many-SC 프로그래밍 모델 연구), PI, Samsung Electronics, 286,000,000 KRW, November 2013 – November 2016
14. An Educational Program for Multicore Programming Experts using Domestic Supercomputer Chundoong (국산 슈퍼컴 "천둥"을 활용한 멀티코어 프로그래밍 전문가 과정), PI, Small and Medium Business Administration (중소기업청/취업연계 R&D 교육센터운영사업/(사)중소기업기술혁신협회), 343,200,000 KRW, April 2015 – December 2015

RESEARCH GRANTS (cont'd) (1.00 USD = 1,111 KRW as of January 2019)

15. Optimization Techniques of JavaScript for Web Applications (웹 애플리케이션을 위한 자바스크립트 최적화 연구), PI, LG Electronics, 90,000,000 KRW, December 2014 – December 2015
16. OpenCL-based Cryptographic Library (OpenCL 기반 암호 라이브러리), PI, Korea Institute of Information Security and Cryptology (한국정보보호학회), 45,000,000 KRW, February 2015 – November 2015
17. Performance Enhancement Techniques using OpenCL (OpenCL 을 활용한 성능향상 기술 개발), PI, Hancom Inc. ((주)한글과 컴퓨터), 100,000,000 KRW, October 2014 – September 2015
18. Core Technology Development for HMA-based System Optimizations (HMA 기반의 시스템 최적화를 위한 요소 기술 개발), Co-PI, Samsung Electronics, 1,200,000,000 KRW, July 2012 – September 2015 (with Hyeonsang Eom (PI) *et al.*)
19. An Educational Program for Multicore Programming Experts using Domestic Supercomputer Chundoong: From Mobile Devices to Supercomputers ([모바일 기기부터 슈퍼컴퓨터까지] 국산 슈퍼컴 "천둥"을 활용한 멀티코어 프로그래밍 전문가 과정), PI, Small and Medium Business Administration (중소기업청/취업연계 R&D 교육센터운영사업/(사)중소기업기술혁신협회), 325,000,000 KRW, May 2014 – December 2014
20. Optimizing OpenCL-based Cryptographic Algorithms for GPUs (GPU 를 위한 OpenCL 기반 암호 알고리즘 최적화), PI, Korea Institute of Information Security and Cryptology (한국정보보호학회), 45,000,000 KRW, February 2014 – November 2014
21. Development of the Big Data Processing Platform based on Manycore Performance Acceleration (매니코어 성능가속형 빅데이터 처리 플랫폼 개발), PI (with ManyCoreSoft Co., Ltd.), Small and Medium Business Administration (중소기업청/산학연 첫걸음기술개발사업), 89,827,000 KRW, July 2013 – June 2014
22. Detailed Planning of Developing Domestic Supercomputing System and Utilization Strategy (국산 초고성능컴퓨팅 시스템 자체개발 및 활용체계 수립 상세 기획), PI, Ministry of Science, ICT and Future Planning (미래창조과학부 기초원천연구기획과제), 60,000,000 KRW, September 2013 – January 2014
23. High Performance Computing Devices (고성능 연산장치 용역연구), PI, Ministry of National Defense (국방부/국군 제 3707 부대, 용역연구), 48,456,822 KRW, September 2013 – December 2013
24. Educational Programs for Parallel Processing Experts using Domestic Supercomputer Chundoong (국산 슈퍼컴 "천둥"을 활용한 병렬 프로그래밍 전문가 과정), PI, Small and Medium Business Administration (중소기업청 / 취업연계 R&D 교육센터운영사업 / (사)중소기업기술혁신협회), 320,000,000 KRW, April 2013 – December 2013
25. Software Techniques for Power Consumption Reduction in Asymmetric Multicore Mobile Platforms (비대칭 멀티코어 모바일 플랫폼의 전력소모 감소를 위한 소프트웨어 기법), PI, Samsung Electronics, 50,000,000 KRW, November 2012 – April 2014
26. Planning and Pilot Study for Establishing Big Data Center (빅 데이터 센터 설립을 위한 기획 및 시범 연구), Co-investigator, Seoul National University, 150,000,000 KRW, November 2012 – October 2013 (with Sungzoon Cho (PI) *et al.*)
27. Memory Footprint Reduction for Tizen Platform and Analysis and Improvement of the Structure of Web-runtime (Tizen 플랫폼의 메모리 사용량 최적화 및 Web-runtime 관련 구조 분석 및 개선안 연구), PI, Samsung Electronics, 120,000,000 KRW, July 2012 – September 2013

RESEARCH GRANTS (cont'd) (1.00 USD = 1,111 KRW as of January 2019)

28. OpenCL Support for ARM Processors (ARM 프로세서를 위한 OpenCL 지원), PI, Samsung Electronics, 100,000,000 KRW, August 2012 – June 2013
29. OpenCL Runtime and Compiler for SRP (SRP 를 위한 OpenCL 런타임 및 컴파일러의 개발), PI, Samsung Electronics, 90,000,000 KRW, April 2012 – April 2013
30. Preliminary Research for Performance Acceleration Programming Models and Parallel Processing Technologies (성능 가속 병렬 프로그래밍 모델 및 병렬처리 기술 선행 연구), PI, Ministry of Knowledge Economy (지식경제부/산업원천기술개발사업/한국전자통신연구원, 위탁연구), 30,000,000 KRW, July 2011 – January 2012
31. Optimizing Browser's JavaScript for Multicore Embedded Platforms (멀티코어 임베디드 플랫폼을 위한 브라우저의 JavaScript 최적화), PI, Samsung India, 76,040,145 KRW, August 2010 – March 2011
32. Designation of an APP Creation Site and Its Management (앱 창작터 지정 운영 사업), Co-investigator, Small and Medium Business Administration (중소기업청), 100,000,000 KRW, May 2010 – December 2010 (with Sang-Goo Lee (PI) *et al.*)
33. Smart Linkers for Mobile Phones (Mobile Phone 환경을 위한 Smart Linker 개발), PI, Samsung Electronics, 70,000,000 KRW, April 2009 – October 2009
34. OpenCL Runtimes and Compilers for Multicore Platforms (멀티코어 플랫폼을 위한 OpenCL 런타임 및 컴파일러의 개발), PI, Samsung Electronics, 150,000,000 KRW, March 2009 – December 2009
35. Executable Image Partitioning and Transformation Techniques for Security (보안을 위한 실행이미지 분할 및 변환 기술에 대한 연구), PI, INNOACE Co., Ltd., (SK 텔레콤/이노에이스(주)), 100,000,000 KRW, December 2008 – December 2009
36. Multisensor-Based Cognitive Information Processing Technologies for Human-Machine Interaction (오감기반 상호인지 정보처리 구현기술), Co-investigator, Ministry of Education, Science and Technology (교육과학기술부/나노원천기술개발사업 / 한국과학재단), 30,000,000 KRW, October 2008 – April 2009 (with Byoung-Tak Zhang (PI) *et al.*)
37. Innovating Software Education with Open Source Software (공개 SW 기반 SW 교육 혁신 프로젝트), Co-investigator, Ministry of Knowledge Economy (지식경제부/한국소프트웨어진흥원), 152,000,000 KRW, October 2008 – December 2010 (with Hyoung-Joo Kim (PI) *et al.*)
38. Analysis of Memory Access Patterns of Operating Systems and Applications in Multicore Server Environments (멀티코어 서버 환경에서 운영체제 및 응용프로그램의 메모리 참조 패턴 분석), PI, Samsung Electronics, Korea. 115,000,000 KRW, May 2008 – December 2010
39. Memory Optimization Techniques for Coarse-Grained Reconfigurable Processors (Coarse-Grained Reconfigurable Processor 를 위한 메모리 최적화 기법), PI, Samsung Electronics, Korea. 120,000,000 KRW, June 2008 – February 2010
40. Development of Flash Memory-based Embedded Multimedia Software (Flash Memory 기반 임베디드 멀티미디어 소프트웨어 기술 개발), Co-investigator, Ministry of Knowledge Economy (지식경제부/IT 핵심기술개발사업/정보통신연구진흥원), 2,980,000,000 KRW, March 2006 – February 2009 (with Sang Lyul Min (PI) *et al.*)
41. Dynamic Voltage and Frequency Scaling Techniques based on Process Characteristics and Automatic Software Development Tools for the Techniques (프로세스 특성에 따른 Voltage 및 Frequency 동적 조절 기법의 개발과 그 적응을 위한 자동화 도구의 개발), PI, Samsung Electronics, 80,000,000 KRW, January 2008 – November 2008

RESEARCH GRANTS (cont'd) (1.00 USD = 1,111 KRW as of January 2019)

42. Embedded Software Optimization using Compiler Techniques (컴파일러 기술을 이용한 임베디드 SW 최적화 기법 연구), PI, Electronics and Telecommunications Research Institute (한국전자통신연구원), 30,000,000 KRW, September 2007 – January 2008
43. Memory Hierarchy Management for Reconfigurable Processors (재구성 가능한 프로세서를 위한 메모리 계층구조 관리 기법), PI, Samsung Electronics, 60,000,000 KRW, December 2006 – November 2007
44. Dual Processor Design Techniques for Mobil Devices, PI, Ministry of Information and Communication (정보통신부), 160,000,000 KRW, April 2006 – November 2007
45. A Target Independent Cross Compilation Environment for Mobile Devices (모바일 단말을 위한 타겟 크로스 컴파일 환경 연구), PI, Electronics and Telecommunications Research Institute (한국전자통신연구원), 30,000,000 KRW, September 2006 – January 2007
46. Embedded S/W Design and Verification Techniques for MPSoC, Co-investigator with Soonhoi Ha (PI) *et al.*, Ministry of Information and Communication, 2,930,000,000 KRW, March 2005 – February 2007
47. Developing a DRAM Test Program and an Operating System that are Optimized for Chip Multiprocessors (Chip Multiprocessor 에 최적화된 메모리 테스트 프로그램 및 이를 위한 운영체제 환경의 개발), PI with Jongmoo Choi, SAMSUNG Electronics, 70,000,000 KRW, January 2006 – December 2006
48. Low Power and High Performance Embedded Video Processors (저전력 고성능 임베디드 비디오 프로세서), Co-investigator with Soo-Ik Chae (PI) and Suhwan Kim, Ministry of Information and Communication, 324,000,000 KRW, April 2004 – February 2006
49. Automatic Code Overlays and Mask ROM Patching using Compiler Techniques (컴파일러 기술을 이용한 Code Overlay 및 Mask ROM Patch 자동화), PI, SAMSUNG Electronics, 60,000,000 KRW, January 2005 – December 2005
50. Developing an Efficient DRAM Test Program Optimized for the 32/64-bit Computing Environment (32/64 비트 환경에 최적화된 고효율 메모리 테스트 프로그램 개발), Co-investigator with Jongmoo Choi (PI), Samsung Electronics, 50,000,000 KRW, December 2004 – November 2005
51. Application Specific and Automatic Power Management Based on Whole Program Analyses, Co-investigator with Heonsik Shin (PI), Microsoft, USA, $30,000, July 2003 – June 2004
52. A Compiler for Helper Threads, CAREER Award, National Science Foundation, USA. Awarded but withdrawn before finalization due to the movement to Seoul National University, Korea. PI, May 2003 – May 2008
53. An Optimizing Compiler for Languages with Programmable Memory Models, Co-PI, Information Technology Research Program, CCR-0081265, National Science Foundation, USA, $499,387, September 2000 – August 2003 (with David A. Padua(PI) and Samuel P. Midkiff)
54. A Proxy Centric Testbed for Mobile Internet Research, Co-PI, CISE Research Resources Program, EIA-0130724, National Science Foundation, USA, $96,390, January 2002 – December 2004 (with Betty H. Cheng, Laura Dillon, Sandeep S. Kulkarni, Philip K. McKinley, and Kurt Stirewalt)

PROFESSIONAL ACTIVITIES

Editorial Board

Journal of Parallel and Distributed Computing — Oct 2015 – Present
ACM Transactions on Parallel Computing (guest editor) — 2019
Journal of Korean Institute of Information Scientists and Engineers — Jan 2008 – Feb 2016

Steering Committee Member

International Conference on High Performance Computing in Asia-Pacific Region — Jan 2017 – Present
ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems — Apr 2010 – Mar 2015

Organizer

HPCAsia '20: International Conference on High Performance Computing in Asia-Pacific Region
Program co-chair, Jan 2020, Fukuoka, Japan

PACT '18: IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques
Publicity co-chair, Nov 2018, Limassol, Cyprus

Accelerator Programming Summer School (가속기 프로그래밍 여름학교)
Principal, Aug 21 – 25, 2017, Aug 20 – 24, 2018
Kumho Asiana HRD Institute (금호아시아나 인재개발원), Yongin, Korea

Accelerator Programming Winter School (가속기 프로그래밍 겨울학교)
Principal, Feb 20 – 24, 2017, Feb 19 – 23, 2018
Lotte Academy (롯데 인재개발원), Osan, Korea
Principal, Feb 18 – 22, 2013
Daekyo HRD Center (대교 HRD 센터), Siheung, Kyungkido, Korea

National Supercomputing Summer School @ SNU (Accelerator Programming)
Principal, Aug 22 – 26, 2016, August 17 – 21, 2015
Kumho Asiana HRD Institute (금호아시아나 인재개발원), Yongin, Korea
Principal, Aug 11 – 14, 2014, August 19 – 22, 2013
Daelim Education and Research Institute (대림교육연구원), Yongin, Korea

National Supercomputing Winter School @ SNU (Accelerator Programming)
Principal, Feb 22 – 26, 2016, Feb 9 – 13, 2015, Feb 10 – 14, 2014
Kumho Asiana HRD Institute (금호아시아나 인재개발원), Yongin, Korea

ISCA'16: The 43rd ACM/IEEE International Symposium on Computer Architecture
Local arrangement chair, Jun 18 – 22, 2016, Seoul, Korea

ICPADS: IEEE International Conference on Parallel and Distributed Systems
Program co-chair (with Sam Midkiff), The 19th, Dec 2013, Seoul, Korea
Vice program co-chair (with Chung-Ping Chung)
Multicore Computing and Parallel/Distributed Architecture track, The 17th, Dec 2011, Tainan, Taiwan
Vice program co-chair (with Ninghui Sun)
Multicore Computing and Parallel/Distributed Architecture track, The 15th, Dec 2009, Shenzhen, China

APSys '12: Asia-Pacific Workshop on Systems
Vice chair, Jul 2012, Seoul, Korea

Cluster '12: IEEE International Conference on Cluster Computing
Vice program chair, Communication and Memory track, Sep 2012, Beijing, China

PROFESSIONAL ACTIVITIES (cont'd)

Organizer (cont'd)

INTERACT: Workshop on Interaction between Compilers and Computer Architectures
General chair, The 16th, Feb 2012, New Orleans, Louisiana, USA
Program co-chair (with Gayatri Mehta), The 15th, Feb 2011, San Antonio, Texas, USA

Heterogeneous Computing Summer School
Co-organizer (with Dongwoo Sheen and Jysoo Lee), Aug16 – 27, 2011
Hanbada Training Center (한바다 연수원), Gapyeong, Kyungkido, Korea

Heterogeneous Computing Winter School
Organizer Feb 21 – 24, 2011
Small Business Training Center (중소기업 연수원), Ansan, Kyungkido, Korea

CF: ACM International Conference on Computing Frontiers
Publicity co-chair, May 2011, Ischia, Italy

LCTES: ACM Conference on Languages, Compilers and Tools for Embedded Systems
General chair, Apr 2010, Stockholm, Sweden
Publicity chair, Jun 2007, San Diego, California, USA

Dagstuhl Seminar 03431: Hardware and Software Consistency Models: Programmability and Performance
Co-organizer (with Sam Midkiff and David A. Padua), October 2003, Germany

JVM: USENIX Java Virtual Machine Research and Technology Symposium
Work-In-Progress session organizer, Aug 2002, San Francisco, CA, USA

Program Committee (PC) member

APPLC: Asia-Pacific Programming Languages and Compilers Workshop (2012, 2013)

APPT: Advanced Parallel Processing Technology Symposium (2011)

CASES: International conference on Compilers, Architecture, and Synthesis for Embedded Systems (2017, 2018, 2019)

CC: International Conference on Compiler Construction (2019)

CGO: International Symposium on Code Generation and Optimization (2016, 2018)

EMSoft: ACM SIGBED Conference on Embedded Software (2006, 2007)

EUC: IFIP International Conference on Embedded and Ubiquitous Computing (2006, 2008, 2009, 2010)

Euro-Par: International European Conference on Parallel and Distributed Computing
Accelerator Computing for Advanced Applications track (2018)

GPGPU: Workshop on General Purpose Processing on Graphics Processing Units (2012)

HiPC: IEEE International Conference on High Performance Computing (2008, 2009)

HiPEAC: European Network of Excellence on High Performance and Embedded Architecture and Compilation Conference
Distinguished reviewer for ACM TACO (2013, 2014, 2015, 2016, 2017, 2018)

HPCAsia: International Conference on High Performance Computing in Asia-Pacific Region
Programming Models and Systems Software track (2018, 2019)

ICPADS: The 12th International Conference on Parallel and Distributed Systems (2006)

ICPP: International Conference on Parallel Processing
Multicores and Parallel Systems track (2011)
Software Systems and Tools track (2008)

PROFESSIONAL ACTIVITIES (cont'd)

Program Committee (PC) member (cont'd)

ICS: ACM International Conference on Supercomputing (2009, 2012, 2013, 2014, 2017)
INTERACT: Workshop on Interaction between Compilers and Computer Architectures (2010)
IPDPS: IEEE International Parallel and Distributed Processing Symposium (2008, 2013, 2014, 2015, 2019)
ISPAN: International Symposium on Parallel Architectures, Algorithms, and Networks (2002)
ISC High Performance, Research Posters (2017)
JVM: USENIX Java Virtual Machine Research and Technology Symposium (2002)
LCPC: International Workshop on Languages and Compilers for Parallel Computing (2017)
LCTES: ACM Conference on Languages, Compilers, and Tools for Embedded Systems (2007, 2008, 2011, 2013)
MICRO: Annual IEEE/ACM International Symposium on Microarchitecture (2018)
Micro Top Picks: IEEE Micro Top Picks (2018)
MSPC: ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (2013)
PACT: IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (2007, 2011, 2012, 2014, 2016, 2017, 2019)
PPoPP: ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (2011, 2017)
RTSS: IEEE Real-Time Systems Symposium
Design and Verification track (2010)
SC: International Conference for High Performance Computing, Networking, Storage and Analysis
Programming Systems track (2012, 2013, 2016, 2017, 2018)
Emerging Technologies track (2015)
Research Posters (2016, 2017)

External Review Committee (ERC) member

HPCA: IEEE Symposium on High Performance Computer Architecture (2016)
ISCA: International Symposium on Computer Architecture (2014, 2015)
MICRO: Annual IEEE/ACM International Symposium on Microarchitecture (2012)
PLDI: ACM SIGPLAN Conference on Programming Language Design and Implementation (2011, 2018)
PPoPP: ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (2013, 2018)

Other Committees

External Ph.D. Thesis Committee (Yan Solihin), Dept. of Computer Science, UIUC, 2002

Member of

IEEE (fellow)
ACM (professional member)
The Korean Institute of Information Scientists and Engineers (KIISE)

INVITED PANELS

College Education Innovation Plans for the 4th Industrial Revolution Oct 2016
Subcommittee of College Education Innovation/Educational Policy Advisory Committee/Ministry of Education
Library of Korean Congress, Seoul
(제 4 차 산업혁명 대비 대학교육혁신 방안, 교육부/교육정책자문위원회/대학교육개혁분과, 국회도서관 소회의실)

Predicting the Form of Next Generation Mobile Devices Jul 2008
Samsung Future Mobile Forum, Samsung Electronics, Korea

Grand Challenges in Embedded Software Oct 2007
EMSoft '07: The 7th ACM Conference on Embedded Software, Salzburg, Austria

TUTORIALS

SnuCL: A Unified OpenCL Framework
PPoPP '14: ACM SIGPLAN 2014 Symposium on Principles and Practice of Parallel Programming, February 2014, Orlando, Florida, USA

OpenCL for Heterogeneous Clusters
ISC '13: International Supercomputing Conference, June 2013, Leipzig, Germany

SnuCL: An OpenCL Framework for Heterogeneous Clusters
ICS '13: ACM International Conference on Supercomputing, June 2013, Eugene, Oregon, USA
PACT '13: The 22nd IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques, September 2013, Edinburgh, Scotland

SnuCL: An OpenCL Framework for Heterogeneous CPU/GPU Clusters
CGO '12: International Symposium on Code Generation and Optimization, March 2012, San Jose, California, USA
ICS '12: ACM International Conference on Supercomputing, June 2012, Venice, Italy
PLDI '12: ACM SIGPLAN 2012 Conference on Programming Language Design and Implementation, June 2012, Beijing, China
PPoPP '12: ACM SIGPLAN 2012 Symposium on Principles and Practice of Parallel Programming, February 2012, New Orleans, Louisiana, USA

SnuCL: An OpenCL Framework and Unified Programming Model for Heterogeneous CPU/GPU Clusters
PACT '11: The 20th IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques, October 2011, Galveston Island, Texas, USA
KCC '11: Korea Computer Congress, June 2011, Kyungju, Korea

INVITED TALKS

Compilers Oct 29, 31, and Nov 2, 2018 (3 days)
Device Solutions Division, Samsung Electronics, Osan, Korea

The Future World Changed by Computer Science and Engineering Sep 2018
(앞으로 컴퓨터공학이 바꾸는 세상)
Jinsung High School, Kwangmyung, Gyeonggi-do, Korea

The Trend of Heterogeneous Systems for Deep Learning Applications Jun 2018
(Deep Learning Application 에 대한 이종 시스템의 동향)
Korea Credit Bureau, Seoul Korea

Target Independent Runtime System for Heterogeneous Accelerators
International Symposium on Future of High Performance Green Computing, Waseda University, Tokyo, Japan Mar 2018
Device Solutions division, Samsung Electronics, Osan, Korea Feb 2018

An HPC Perspective on PIM Systems
Device Solutions, Samsung Electronics, Osan, Korea Jan 2018
Memory division, Device Solutions, Samsung Electronics, Osan, Korea Aug 2017

Heterogeneous Computing in Post Moore's Era Dec 2017
Electronics and Telecommunications Research Institute, Daejeon, Korea

INVITED TALKS (cont'd)

The Adventure of an 11th Graduate from Jinsung High School to Deep Learning Nov 2017
(진성고등학교 11 기 졸업생의 딥 러닝을 향한 도전)
Jinsung High School, Kwangmyung, Gyeonggi-do, Korea

An HPC Perspective on Deep Learning Nov 2017
Korea Supercomputing Conference, Seoul, Korea

Scalable Heterogeneous Programming Models for Deep Learning Applications Jan 2017
Software Convergence Symposium, Seoul, Korea

OpenCL Programming Model for FPGAs Jan 2017
Winter Workshop, SIG on Computer Systems, The Korean Institute of Information Scientists and Engineers

Scalable Heterogeneous Programming Models for Deep Learning Applications
ACM SIGARCH Korea Chapter Workshop (Keynote) Oct 2016
WASEA – Workshop on Architecture and Software for Emerging Applications (PACT '16) Sep 2016

Foundational Skills and User Lock-in (기본기와 사용자 Lock-in) Nov 2015
S/W Future Vision 2020, Software Center, R & D Center, Samsung Electronics, Suwon, Korea

Introduction to Computer Science Jan 2015 (3 days), Jul 2014 (3 days), Jan 2014 (3 days), Jul 2013 (2 days)
Samsung Convergence Software Academy, Samsung SDS, Seoul, Korea

Software Basics Jan 2015 (2 days), Jul 2014 (2 days), Jan 2014 (2 days), Jul 2013 (2 days)
Samsung Convergence Software Academy, Samsung SDS, Seoul, Korea

The Design of Water-Cooled HPC Systems and Their Application Parallelization and Optimizations Dec 2014
Semiconductor Division, Samsung Electronics, Yongin, Korea

Software Development for Embedded Multicore Systems Apr 2014 (3 days), Jul 2013 (3 days), Apr 2013 (3 days)
Samsung Advanced Technology Training Institute, Suwon, Korea

Compiler Optimization Techniques Dec 2013
DS division, Samsung Electronics, Korea

Code Optimization Techniques Jul 2013 (3 days)
Samsung Advanced Technology Training Institute, Suwon, Korea

Heterogeneous Computing and Software Issues May 2013
System LSI division, Samsung Electronics, Korea

A Small but Powerful Supercomputer Chundoong and Its Programming Model Jan 2013
Winter Workshop, SIG on Computer Systems, The Korean Institute of Information Scientists and Engineers

Introduction to Multicores Nov 2012
Digital Media & Communications R & D Center, Samsung Electronics, Korea

Introduction to Parallel Software Development
Device Solutions division, Samsung Electronics, Korea Nov 2012
Samsung Advanced Technology Training Institute, Suwon, Korea Sep 2012

Compilers Mar 2012
DS division, Samsung Electronics, Korea

SnuCL: An OpenCL Vehicle for Heterogeneous Computing Dec 2011
Korea University

Architectures and Programming Models for Heterogeneous Parallel Computing Nov 2011
Samsung Multicore Forum, Samsung Advanced Institute of Technology, Korea

OpenCL as a Programming Model for Large Scale Heterogeneous Computing Nov 2011
International Workshop on Exascale Supercomputing

INVITED TALKS (cont'd)

Programming Models for Heterogeneous Computing Oct 2011
Dept. of Computer Science, Korea Advanced Institute of Science and Technology

Trends and Issues in Heterogeneous Computing Sep 2011
Samsung Advanced Technology Training Institute, Suwon, Korea

Software Development for Embedded Multicore Systems Sep 2011 (3 days)
Samsung Advanced Technology Training Institute, Suwon, Korea

SnuCL: An OpenCL Framework and Unified Programming Model for Heterogeneous CPU/GPU Clusters Jul 2011
Fudan University, Shanghai, China

OpenCL as a Unified Programming Interface for CPU-GPU Clusters Jan 2011
KISTI (Korea Institute of Science and Technology Information), Daejeon, Korea

Multicore Software Development Nov 2010 (2 days)
Samsung Advanced Technology Training Institute, Suwon, Korea

A Software SVM Approach for Heterogeneous Multicore Accelerator Clusters May 2010
Multicore/GPU Computing Workshop, KIAS (Korea Institute for Advanced Study)
The Korean Society for Computational Sciences and Engineering, Korea

Introduction to OpenCL
Korea Institute of Science and Technology, Seoul, Korea Feb 2010
Samsung India Software Operations, Bangalore, India Sep 2009

Software SVM Approach for Heterogeneous Accelerator Multicore Architectures
Winter Workshop, Special Interest Group on Computer Systems, KIISE, Korea Jan 2010
Samsung India Software Operations, Bangalore, India Jan 2010

Parallel Programming Models and OpenCL in the Multicore Era Nov 2009
Samsung Multicore Forum, Samsung Advanced Institute of Technology, Korea

Compilers and Runtimes Support for Explicitly Managed Memory Hierarchies Jul 2009 (5 days, 1 lecture/day)
ACACES '09: the fifth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems, Terrassa, Spain

FaCSim: A Fast and Cycle-Accurate Architecture Simulator for Embedded Systems Nov 2008
Digital Media Division, Samsung Electronics, Korea

COMIC: A Coherent Shared Memory Interface for Cell BE
Samsung Advanced Institute of Technology, Korea Dec 2008
School of Computer Science, Georgia Institute of Technology, Atlanta, USA Oct 2008
IBM T. J. Watson Research Center, Hawthorne, New York, USA Oct 2008

Multicore Programming Models Sep 2008
Telecommunication Network Division, Samsung Electronics, Korea

Issues in Parallel Programming Models for Multi/Manycores Aug 2008
Samsung Advanced Institute of Technology, Korea

Hiding Relaxed Memory Consistency with Compilers Feb 2008
School of Computing, University of Utah, Salt Lake City, Utah, USA

Virtual Memory Environments for Instruction Scratchpad Memory Management Mar 2007
Dagstuhl Seminar 07101: Quantitative Aspects of Embedded Systems, Schloss Dagstuhl, Wadern, Germany

Memory Hierarchy Optimization in Software Dec 2004
Memory Division, Samsung Electronics, Korea

New Optimization Opportunities for Embedded Software Dec 2004
National Chiao Tung University, Taiwan

INVITED TALKS (cont'd)

What can Compilers do for Embedded Systems? Mar 2004
Samsung Software Center, Samsung Electronics, Korea

Software Memory Consistency Models Nov 2003
Fall Conference, SIG on Programming Languages, KIISE

Advanced Compiler Technologies Aug 2003
Embedded Systems Session, European Summer School on Embedded Systems, Mälardalen University, Sweden

Performance Improvement of Processing-In-Memory Systems by Using Memory Threads
Korea University, Seoul, Korea Nov 2002
System LSI Division, Samsung Electronics, Korea Oct 2002

Automatically Mapping Code on an Intelligent Memory Architecture Feb 2001
Department of Electrical and Computer Engineering, Northwestern University, IL, USA

An Optimizing Compiler for Relaxed Memory Consistency Models
Department of Computer Science, University of Massachusetts at Amherst, MA, USA Feb 2001
Department of Computer Science, Northwestern University, IL, USA Feb 2001
Department of Computer Science, State University of New York at Stony Brook, NY, USA Mar 2001
Department of Computer Science, Boston University, MA, USA Mar 2001

Compilation Techniques for Explicitly Parallel Programs
Dagstuhl Seminar 00341: High Performance Computing and Java, Schloss Dagstuhl, Wadern, Germany Aug 2000
School of Computer Science and Engineering, Seoul National University, Korea May 2000
Department of Electrical and Computer Engineering, University of Toronto, Canada July 1999
Star Core, Atlanta, GA, USA Jun 1999
Intel, Santa Clara, CA, USA Apr 1999
Sun Microsystems, Mountain View, CA, USA Apr 1999
Hewlett Packard, Cupertino, CA, USA Apr 1999
Department of Computer Science, University of Rochester, NY, USA Mar 1999
Department of Computer Science and Engineering, Michigan State University, MI, USA Mar 1999
Department of Computer Science, Florida State University, Tallahassee, FL, USA Mar 1999

STUDENTS

Current Ph.D. Students

Jungho Park (박정호), Yong-Jun Lee (이용준), Hongjune Kim (김홍준), Gangwon Jo (조강원), Thanh Tuan Dao (다오 탄 투안), Wookeun Jung (정우근), Jaehoon Jung (정재훈), Heehoon Kim (김희훈), Hyungmo Kim (김형모), Youngdong Do (도영동),

Graduated Ph.D. Students

Junghyun Kim (김정현) Febr 2016
Thesis: Techniques for Ease of OpenCL Programming
Senior Research Staff Member, Software Center, Samsung Electronics

Sangmin Seo (서상민) Aug 2013
Thesis: Enhancing Performance Portability of OpenCL for Multicore CPUs
Senior Research Staff Member, Software Center, Samsung Electronics

Jungwon Kim (김정원) Aug 2013
Thesis: An OpenCL Framework for Heterogeneous Clusters
Computer Scientist, Oak Ridge National Laboratory, USA

Choonki Jang (장춘기) Aug 2011
Thesis: Optimization and Management Techniques for Local Memory Architectures
Senior Research Staff Member, Samsung Advanced Institute of Technology

Bernhard Egger (이강웅) Feb 2008
Thesis: Dynamic Scratchpad Memory Management
Associate Professor, Department of Computer Science and Engineering, SNU

Current M.S. Students

Jungwook Kim (김정욱), PyeongSeok Oh (오평석), Janghyun Son (손장현), and Daeyoung Park (박대영)

Graduated M.S. Students

Jiyoung Park (박지영), TMaxSoft Feb 2018
Thesis: FPGA Accelerator Design of a Deep Reinforcement Learning Model for Playing Atari Games

Jaeho Shin (신재호), SKHynix Feb 2017
Thesis: Auto-optimization of Image Processing Programs using OpenCL through Dynamic Workload Distribution

Bojun Seo (서보준), LG Electronics Aug 2016
Thesis: Reducing Memory Usage by Sharing Code on V8 JavaScript Engine

Jinyoung Joo (주진영), TmaxSoft Aug 2014
Thesis: Bi-directional Source-to-Source Translator between CUDA and OpenCL

Seonmyeong Bak (박선명), Ph.D. student at UIUC, USA Aug 2014
Thesis: Lightweight Block-level Concurrent Wweeping for JavaScript Garbage Collection

Jeongho Nah (나정호), TmaxSoft Feb 2012
Thesis: Implementation of a Reigster Allocator for a JavaScript JIT Compiler

Joo Hwan Lee (이주환), Samsung Research America, USA Aug 2011
Thesis: Reducing JavaScript Compilation Time by Caching Code in Flash Memory

Eunbyung Park (박은병), Ph.D student at UNC Chapel Hill, USA Feb 2011
Thesis: Fast and Space-Efficient Virtual Machine Checkpointing

STUDENTS (cont'd)

Graduated M.S. Students (cont'd)

Honggyu Kim (김홍규), LG Electronics, Korea Feb 2010
Thesis: Adaptive Execution Techniques of Parallel Programs for SMT Multicore

Jinho Pak (박진호), NCsoft, Korea Feb 2010
Thesis: The Design and Implementation of UI for Architecture Simulator

Junghyun Kim (김정현), Ph.D. student, SNU Feb 2009
Thesis: The Design and Implementation of Parallelized Architecture Simulator for Embedded Systems

Posung Chun (전보성), TmaxSoft Feb 2009
Thesis: Coherent Distributed Shared Memory Interface for Cell BE Cluster

Taejun Ha (하태준), TmaxSoft Feb 2008
Thesis: An Automatic Memory Subsystem Parameter Detection Program

Chihun Kim (김지훈), Nexon Feb 2008
Thesis: A Dynamic Code Placement Technique for Scratchpad Memory Using Postpass Optimization

Kwangsub Kim (김광섭), LG Electronics Feb 2008
Thesis: Optimization Techniques for Cycle-Accurate Instruction Set Simulator

Yoonsung Nam (남윤성), Samsung Electronics Feb 2007
Thesis: Cycle-Accurate and Fast Simulation Techniques for ARM Processors

Jongyoung Lee (이종영), Samsung Electronics Aug 2006
Thesis: Reducing Execution Time of Memory Test Programs using SIMD Instructions and Caches in 64-bit Computing Environments

Seokho Choi (최석호), SKY Teletech Aug 2005
Thesis: An Intermediate Representation for Preserving Source Level Information and Optimization

Kiwon Kwon (권기원), Qualcomm, Korea Feb 2005
Thesis: SNACK-pop: A Postpass Optimizer for Embedded Systems

Changhee Jung (정창희), Assistant Professor, Virginia Tech, USA Feb 2005
Thesis: Helper Thread Prefetching for a Loosely-Coupled Multiprocessor System

Xing Fang (at MSU), Software Development Engineer, Amazon, USA Aug 2002
Thesis: Inserting Fences to Guarantee Sequential Consistency

H. D. K. Moonesinghe (at MSU) Aug 2002
Thesis: Adaptively Increasing Performance and Scalability of Automatically Parallelized Programs

COURSES TAUGHT

Graduate Courses at SNU

4541.775 Topics in Compiler Construction	Fall 2003, 2004, 2005, 2006, 2007
4541.570 Advanced Compiler Construction	Spring 2006, 2007, 2010

Graduate Courses at Michigan State University

CSE 891 Advanced Program Analysis and Optimization Techniques	Fall 2001
CSE 822 Parallel Processing Computer Systems	Spring 2001

Undergraduate Courses at SNU

010.133 Digital Computer Concept and Practice	Spring 2010, 2011, 2012, 2013
010.143 Computer Principles	Spring 2008
M1522.000700 Logic Design	Spring 2018
400.313 Field Applications of Engineering Knowledge	Fall 2017
4190.101 Discrete Mathematics	Spring 2003, 2004, 2005
4190.103 Programming Practice	Summer 2008, Fall 2009, Spring 2017, 2018
4190.203 System Programming	Fall 2003, 2004
4190.209 Computer Engineering Seminar	Fall 2009
4190.210 Principles of Programming	Fall 2005, 2006, 2007
4190.310 Programming Languages	Fall 2002, Spring 2014
4190.311A Project 1	Fall 2002
4190.409 Compilers	Spring 2003, 2004, 2005, 2006, 2007, 2008, 2011, 2012
4190.413A Project 2	Fall 2002
4190.414A Multicore Computing	Spring 2013, 2014, 2015, Fall 2016, 2017, 2018
4190.422 IT-leadership Seminar	Spring 2017

Undergraduate Courses at Michigan State University

CSE 320 Computer Organization and Assembly Language Programming	Fall 2000
CSE 450 Translation of Programming Languages	Spring 2000, 2002
CS 231 Computer Architecture I	Fall 1999
CS296 Honors Course in Computer Science	Fall 1999

PUBLICATIONS

Book Chapters

1. Jaejin Lee, Gangwon Jo, Wookeun Jung, Hongjune Kim, Junghyun Kim, Yong-Jun Lee, and Jungho Park. SnuCL: A unified OpenCL framework for heterogeneous clusters, *Advanced in GPU Research and Practice*, pp. 23 — 56, Morgan Kaufmann, September 2016.

Refereed Conference and Workshop Papers

1. Hyungmin Cho, Pyeongseok Oh, Jiyoung Park, Wookeun Jung, and Jaejin Lee. FA3C: FPGA-Accelerated Deep Reinforcement Learning, ***ASPLOS '19***: *Proceedings of the 24th International Conference on Architectural Support for Programming Languages and Operating Systems*, Providence, Rhode Island, USA, April 2019
2. Gangwon Jo, Jaehoon Jung, Jiyoung Park, and Jaejin Lee. Memory-Access-Pattern Analysis Techniques for OpenCL Kernels, ***LCPC '17***: *Proceedings of the 30th International Workshop on Languages and Compilers for Parallel Computing*, College Station, Texas, USA, October 2017
3. Heehoon Kim, Hyoungwook Nam, Wookeun Jung, and Jaejin Lee. Performance Analysis of CNN Frameworks for GPUs, ***ISPASS '17***: *Proceedings of 2017 IEEE International Symposium on Performance Analysis of Systems and Software*, pp. 55 — 64, Santa Rosa, California, USA, April 2017. (24/81, 29.6%)
4. Junghyun Kim, Yong-Jun Lee, Jungho Park, and Jaejin Lee. Translating OpenMP Device Constructs to OpenCL Using Unnecessary Data Transfer Elimination, ***SC '16***: *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, Salt Lake City, Utah, USA, November 2016. (82/446, 18.4%)
5. Jungho Park, Wookeun Jung, Gangwon Jo, Ilkoo Lee, and Jaejin Lee. PIPSEA: A Practical IPsec Gateway on Embedded APUs, ***CCS '16***: *Proceedings of the 23rd ACM Conference on Computer and Communications Security*, Vienna, Austria, October 2016. (137/831, 16.5%)
6. Junghyun Kim, Gangwon Jo, Jaehoon Jung, Jungwon Kim, and Jaejin Lee. A Distributed OpenCL Framework using Redundant Computation and Data Replication, ***PLDI '16***: *Proceedings of the 37th Annual ACM SIGPLAN Conference on Programming Language Design and Implementation*, pp. 553 — 569, Santa Barbara, California, USA, June 2016, DOI: 10.1145/2908080.2908094. (48/304, 15.8%)
7. Junghyun Kim, Thanh Tuan Dao, Jaehoon Jung, Jinyoung Joo, and Jaejin Lee. Bridging OpenCL and CUDA: A Comparative Analysis and Translation, ***SC '15***: *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, Article No. 82, Austin, Texas, USA, November 2015, DOI: 10.1145/2807591.2807621. (79/358, 22.1%)
8. Wookeun Jung, Jongsoo Park, and Jaejin Lee. Versatile and scalable parallel histogram construction, ***PACT '14***: *Proceedings of the 23rd ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 127 — 138, Edmonton, Alberta, Canada, August 2014, DOI: 10.1145/2628071.2628108. (37/144, 25.7%)
9. Hongjune Kim, Seonmyeong Bak, and Jaejin Lee. Lightweight and block-level concurrent sweeping for javascript garbage collection, ***LCTES '14***: *Proceedings of the 2014 SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems*, pp. 155 — 164, Edinburgh, UK, June 2014, DOI: 10.1145/2597809.2597824. (16/51, 31.3%)
10. Gangwon Jo, Won Jong Jeon, Wookeun Jung, Gordon Taft, and Jaejin Lee. OpenCL Framework for ARM Processors with NEON Support, ***WPMVP '14***: *Proceedings of the 2014 Workshop on Programming Models for SIMD/Vector Processing*, pp. 33 — 40, February 2014.

PUBLICATIONS (cont'd)

Refereed Conference and Workshop Papers (cont'd)

11. Sangmin Seo, Jun Lee, Gangwon Jo, and Jaejin Lee. Automatic OpenCL Work-Group Size Selection for Multicore CPUs, ***PACT '13***: *Proceedings of the 22nd ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, Edinburgh, Scotland, September 2013, DOI: 10.1109/PACT.2013.6618834. (36/208, 17.3%)
12. Choonki Jang, Jaejin Lee, Bernhard Egger, and Soojung Ryu. Automatic Code Overlay Generation and Partially Redundant Code Fetch Elimination, Presented in ***HiPEAC '13***: *High Performance and Embedded Architecture and Compilation Conference*, Berlin, Germany, January 2013. (Published in *ACM Transactions on Architecture and Code Optimization*, Vol. 9, No. 2, Article 10, June 2012, DOI:10.1145/2207222.2207226)
13. Jungwon Kim, Sangmin Seo, Jun Lee, Jeongho Nah, Gangwon Jo, and Jaejin Lee. SnuCL: an OpenCL Framework for Heterogeneous CPU/GPU Clusters, ***ICS '12***: *Proceedings of the 26th International Conference on Supercomputing*, pp. 341 — 352, San Servolo Island, Venice, Italy, June 2012, DOI: 10.1145/2304576.2304623. (36/161, 22.3%)
14. Choonki Jang, Jun Lee, Sangmin Seo, and Jaejin Lee. An Automatic Code Overlaying Technique for Multicores with Explicitly-Managed Memory Hierarchies, ***CGO '12***: *Proceedings of the 2012 International Symposium on Code Generation and Optimization*, pp. 219 — 229, San Jose, California, USA, March 2012, DOI: 10.1145/2259016.2259045. (26/90, 28.8%)
15. Sangmin Seo, Gangwon Jo, and Jaejin Lee. Performance Characterization of the NAS Parallel Benchmarks in OpenCL, ***IISWC '11***: *Proceedings of the 2011 IEEE International Symposium on Workload Characterization*, pp. 137 — 148, Austin, Texas, USA, November 2011, DOI: 10.1109/IISWC.2011.6114174. (20/50, 40.0%)
16. Sangmin Seo, Junghyun Kim, and Jaejin Lee. SFMalloc: A Lock-Free and Mostly Synchronization-Free Dynamic Memory Allocator for Manycores, ***PACT '11***: *Proceedings of the 20th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 253 — 263, Galveston Island, Texas, USA, October 2011, DOI: 10.1109/PACT.2011.57. (36/221, 16.3%)
17. Jun Lee, Jungwon Kim, Junghyun Kim, Sangmin Seo, and Jaejin Lee. An OpenCL Framework for Homogeneous Manycores with no Hardware Cache Coherence, ***PACT '11***: *Proceedings of the 20th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 56 — 67, Galveston Island, Texas, USA, October 2011, DOI: 10.1109/PACT.2011.12. (36/221, 16.3%)
18. Jungwon Kim, Sangmin Seo, Jun Lee, Jeongho Nah, Gangwon Jo, and Jaejin Lee. OpenCL as a Programming Model for GPU Clusters, ***LCPC '11***: *Proceedings of the 24th International Workshop on Languages and Compilers for Parallel Computing* (also appears in Springer-Verlag Lecture Notes in Computer Science, Vol. 7146, 2013), pp. 76 — 90, Fort Collins, Colorado, USA, September 2011, DOI: 10.1007/978-3-642-36036-7_6. (19/52, 36.5%)
19. Junghyun Kim, Sangmin Seo, and Jaejin Lee. An Efficient Software Shared Virtual Memory for the Single-chip Cloud Computer, ***APSys '11***: *Proceedings of the 2nd ACM SIGOPS Asia-Pacific Workshop on Systems*, Article No. 4, Shanghai, China, July 2011, DOI: 10.1145/2103799.2103804. (19/57, 33.3%)
20. Choonki Jang, Jungwon Kim, Jaejin Lee, Hee-Seok Kim, Dong-Hoon Yoo, Sukjin Kim, Hong-Seok Kim, and Soojung Ryu. An Instruction-Scheduling-Aware Data Partitioning Technique for Coarse-Grained Reconfigurable Architectures, ***LCTES '11***: *Proceedings of the ACM SIGPLAN/SIGBED 2011 International Conference on Languages, Compilers, and Tools for Embedded Systems*, pp. 151 — 160, Chicago, Illinois, USA, April 2011, DOI: 10.1145/1967677.1967699. (17/51, 33.3%)

PUBLICATIONS (cont'd)

Refereed Conference and Workshop Papers (cont'd)

21. Eunbyung Park, Bernhard Egger, and Jaejin Lee. Fast and Space Efficient Virtual Machine Checkpointing, ***VEE '11***: *Proceedings of the 2011 ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments*, pp. 75 — 85, Newport Beach, California, USA, March 2011, DOI: 10.1145/1952682.1952694. (20/68, 29.4%)
22. Jungwon Kim, Honggyu Kim, Joo Hwan Lee, and Jaejin Lee. Achieving a Single Compute Device Image in OpenCL for Multiple GPUs, ***PPoPP '11***: *Proceedings of the 16th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 277— 288, San Antonio, Texas, USA, February 2011, DOI: 10.1145/1941553.1941591. (26/165, 15.6%)
23. Yongjin Cho, Seungkyun Kim, Jaejin Lee, and Heonshik Shin. Parallelizing the H.264 Decoder on the Cell BE Processor. ***EMSoft '10***: *Proceedings of the 10th ACM International Conference on Embedded Software*, pp. 49 — 58, Scottsdale, Arizona, October 2010. DOI: 10.1145/1879021.1879029. (29/89, 32.6%)
24. Jaejin Lee, Jungwon Kim, Sangmin Seo, Seungkyun Kim, Jungho Park, Honggyu Kim, Thanh Tuan Dao, Yongjin Cho, Sung Jong Seo, Seung Hak Lee, Seung Mo Cho, Hyo Jung Song, Sang-Bum Suh, and Jong-Deok Choi. An OpenCL Framework for Heterogeneous Multicores with Local Memory, ***PACT '10***: *Proceedings of the 19th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 193 — 204, Vienna, Austria, September 2010, DOI: 10.1145/1854273.1854301. (46/266, 17.3%)
25. Jaejin Lee, Jun Lee, Sangmin Seo, Jungwon Kim, Seungkyun Kim, and Zehra Sura. COMIC++: A Software SVM System for Heterogeneous Multicore Accelerator Clusters. ***HPCA '10***: *Proceedings of the 16th IEEE International Symposium on High Performance Computer Architecture*, pp. 329 — 340, Bangalore, India, January 2010, DOI:10.1109/HPCA.2010.5416633. (32/175, 18.3%)
26. Sangmin Seo, Jaejin Lee, and Zehra Sura. Design and Implementation of Software-Managed Caches for Multicores with Local Memory. ***HPCA '09***: *Proceedings of the 15th IEEE International Symposium on High Performance Computer Architecture*, pp. 55 — 66, Raleigh, North Carolina, USA, February 2009, DOI:10.1109/HPCA.2009.4798237. (35/184, 19.0%)
27. Jaejin Lee, Sangmin Seo, Chihun Kim, Junghyun Kim, Posung Chun, Zehra Sura, Jungwon Kim, and SangYong Han. COMIC: A Coherent Shared Memory Interface for Cell BE. ***PACT '08***: *Proceedings of the 17th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 303 — 314, Toronto, Canada, October 2008, DOI:10.1145/1454115.1454157. (30/159, 18.9%)
28. Bernhard Egger, Jaejin Lee, and Heonshik Shin. Scratchpad Memory Management in a Multitasking Environment. ***EMSoft '08***: *Proceedings of the 8th ACM International Conference on Embedded Software*, pp. 265 — 274, Atlanta, Georgia, October 2008, DOI:10.1145/1450058.1450094. (28/110, 25.4%)
29. Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, Kwangsub Kim, and SangYong Han. FaCSim: A Fast and Cycle-Accurate Architecture Simulator for Embedded Systems. ***LCTES '08***: *Proceedings of the ACM SIGPLAN/SIGBED 2008 International Conference on Languages, Compilers, and Tools for Embedded Systems* (also appears in *ACM SIGPLAN Notices*, Vol. 43, No. 7, July 2008), pp. 89 — 99, Tucson, Arizona, USA, June 2008, DOI:10.1145/1379023.1375670. (17/68, 25.4%)

PUBLICATIONS (cont'd)

Refereed Conference and Workshop Papers (cont'd)

30. Hyeongmin Cho, Bernhard Egger, Jaejin Lee, and Heonshik Shin. Dynamic Data Scratchpad Memory Management for a Memory Subsystem with an MMU. ***LCTES '07***: *Proceedings of the ACM SIGPLAN/SIGBED 2007 International Conference on Languages, Compilers*, and Tools for Embedded Systems (also appears in ACM SIGPLAN Notices, Vol. 42, No. 7, July 2007), pp. 195 — 206, San Diego, USA, June 2007, DOI:10.1145/1273444.1254804. (21/76, 27.6%)
31. Bernhard Egger, Jaejin Lee, and Heonshik Shin. Scratchpad Memory Management for Portable Systems with a Memory Management Unit. ***EMSoft '06***: *Proceedings of the 6th ACM International Conference on Embedded Software*, pp. 321 — 330, Seoul, Korea, October 2006, DOI:10.1145/1176887.1176933. (31/94, 33.0%)
32. Bernhard Egger, Chihun Kim, Choonki Jang, Yoonsung Nam, Jaejin Lee, and Sang Lyul Min. A Dynamic Code Placement Technique for Scratchpad Memory using Postpass Optimization. ***CASES '06***: *Proceedings of the 2006 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, pp. 223 — 233, Seoul, Korea, October 2006, DOI:10.1145/1176760.1176788. (25/100, 25.0%)
33. Changhee Jung, Daesub Lim, Jaejin Lee, Yan Solihin. Helper Thread Prefetching for Loosely-Coupled Multiprocessor Systems, ***IPDPS '06***: *Proceedings of the 2006 IEEE International Parallel & Distributed Processing Symposium*, pp. 118 — 127, Rhodes Island, Greece, April 2006, DOI:10.1109/IPDPS.2006.1639375. (125/531, 23.5%)
34. Chi-Leung Wong, Zehra Sura, Xing Fang, Kyungwoo Lee, Samuel P. Midkiff, Jaejin Lee, and David Padua. Evaluating the Impact of Thread Escape Analysis on a Memory Consistency Model-Aware Compiler. ***LCPC '05***: *Proceedings of the 18th International Workshop on Languages and Compilers for Parallel Computing* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 4339, 2007), pp. 170 — 184, Hawthorne, New York, October 2005, DOI:10.1007/978-3-540-69330-7_12.
35. Zehra Sura, Xing Fang, Chi-Leung Wong, Samuel P. Midkiff, Jaejin Lee, and David Padua. Compiler Techniques for High Performance Sequentially Consistent Java Programs. ***PPoPP '05***: *Proceedings of the ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 2 — 13, Chicago, Illinois, USA, June 2005, DOI:10.1145/1065944.1065947. (27/87, 31.0%)
36. Changhee Jung, Daeseob Lim, Jaejin Lee, and SangYong Han. Adaptive Execution Techniques for SMT Multiprocessor Architectures. ***PPoPP '05***: *Proceedings of the ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 236 — 246, Chicago, Illinois, USA, June 2005, DOI:10.1145/1065944.1065976. (27/87, 31.0%)
37. Chanik Park, Junghee Lim, Kiwon Kwon, Jaejin Lee, and Sang Lyul Min. Compiler Assisted Demand Paging for Embedded Systems with Flash Memory. ***EMSoft '04***: *Proceedings of the 4th ACM International Conference on Embedded Software*, pp. 114 — 124, Pisa, Italy, September 2004, DOI:10.1145/1017753.1017775. (31/87, 35.6%)
38. Bernhard Egger, Jaejin Lee, and Heonshik Shin. An Application-Specific and Adaptive Power Management Technique. ***PARC '04***: *Proceedings of the First International Workshop on Power-Aware Real-Time Computing* (in conjunction with *EMSoft '04*), Pisa, Italy, September 2004, http://www.cs.pitt.edu/PARC/parc-6.pdf
39. Sheayun Lee, Jaejin Lee, Chang Yun Park, and Sang Lyul Min. Flexible Tradeoff between Code Size and WCET Using a Dual Instruction Set Processor. ***SCOPES '04***: *Proceedings of the 8th International Workshop on Software and Compilers for Embedded Systems* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 3199, 2004), pp. 244 — 258, Amsterdam, Netherlands, September 2004, DOI:10.1007/b99901. (***Best Paper Award***, 17/50, 34.0%)

PUBLICATIONS (cont'd)

Refereed Conference and Workshop Papers (cont'd)

40. Mazen Kharbutli, Yan Solihin, and Jaejin Lee. Using Prime Numbers for Cache Indexing to Eliminate Conflict Misses. ***HPCA '04***: *Proceedings of the 10th International Symposium on High Performance Computer Architecture*, pp. 288 — 299, Madrid, Spain, February 2004, DOI:10.1109/HPCA.2004.10015. (27/153, 17.6%)
41. Sheayun Lee, Jaejin Lee, Sang Lyul Min, Jason Hiser, and Jack W. Davidson. Code Generation for a Dual Instruction Set Processor Based on Selective Code Transformation. ***SCOPES '03***: *Proceedings of the 7th International Workshop on Software and Compilers for Embedded Systems* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 2826, 2003), pp. 33 — 48, Vienna, Austria, September 2003, DOI:10.1007/b13482. (26/43, 60.5%)
42. Sheayun Lee, Jaejin Lee, Chang Yun Park, and Sang Lyul Min. A Flexible Tradeoff between Code Size and WCET Employing Dual Instruction Set Processors. ***WCET '03***: *Proceedings of the 3rd International Workshop on Worst-Case Execution Time Analysis*, pp. 91 — 94, Porto, Portugal, July 2003.
43. Xing Fang, Jaejin Lee, and Samuel P. Midkiff. Automatic Fence Insertion for Shared Memory Multiprocessing. ***ICS '03***: *Proceedings of the 17th ACM International Conference on Supercomputing*, pp. 285 — 294, San Francisco, Bay Area, USA, June 2003, DOI:10.1145/782814.782854. (36/171, 21.1%)
44. Jaejin Lee. The Pensieve Project: Automatic Implementation of Programming Language Consistency Models. Short talk on Emerging Research Topics session in ***PPoPP '03***: *the ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, Chicago, Illinois, USA, June 2003
45. Jaejin Lee and H. D. K. Moonesinghe. Adaptively Increasing Performance and Scalability of Automatically Parallelized Programs. ***LCPC '02***: *Proceedings of the 15th International Workshop on Languages and Compilers for Parallel Computing* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 2481, 2005), pp. 203 — 217, College Park, Maryland, USA, July 2002, DOI:10.1007/11596110_14.
46. Zehra Sura, Chi-Leung Wong, Xing Fang, Jaejin Lee, Samuel P. Midkiff, and David Padua. Automatic Implementation of Programming Language Consistency Models. ***LCPC '02***: *Proceedings of the 15th International Workshop on Languages and Compilers for Parallel Computing* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 2481, 2005), pp. 172 — 187, College Park, Maryland, USA, July 2002, DOI:10.1007/11596110_12.
47. Ji Zhang, Jaejin Lee, and Philip K. McKinley. Optimizing the Java Pipe I/O Stream Library for Performance. ***LCPC '02***: *Proceedings of the 15th International Workshop on Languages and Compilers for Parallel Computing* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 2481, 2005), pp. 233 — 248, College Park, Maryland, USA, July 2002, DOI:10.1007/11596110_16.
48. Chi-Leung Wong, Zehra Sura, Xing Fang, Samuel P. Midkiff, Jaejin Lee, and David Padua. A Compiler Infrastructure for Memory Models, ***ISPAN '02***: *Proceedings of the 6th International Symposium on Parallel Architectures*, Algorithms,and Networks, pp. 239 — 244, Manila, Philippines, May 2002, DOI:10.1109/ISPAN.2002.1004288
49. Yan Solihin, Jaejin Lee, and Josep Torrellas. Using a User-Level Memory Thread for Correlation Prefetching. ***ISCA '02***: *Proceedings of the 29th Annual International Symposium on Computer Architecture*, pp. 171 — 182, Anchorage, Alaska, USA, May 2002, DOI:10.1109/ISCA.2002.1003576. (27/180, 15.0%)

PUBLICATIONS (cont'd)

Refereed Conference and Workshop Papers (cont'd)

50. Yan Solihin, Jaejin Lee, and Josep Torrellas. Prefetching in an Intelligent Memory ArchitectureUsing a Helper Thread. ***MTEAC-5****: Proceedings of the 5th Workshop on Multithreaded Execution, Architecture and Compilation* (in conjunction with MICRO-34), Austin, Texas, USA, December 2001. (***Best Paper Award***)
51. Samuel P. Midkiff, Jaejin Lee, David A. Padua. A Compiler for Multiple Memory Models. ***CPC '01****: Proceedings of the 9th Workshop on Compilers for Parallel Computers*, Edinburgh, Scotland, UK, June 2001 (http://www.icsa.informatics.ed.ac.uk/cpc2001).
52. Jaejin Lee, Yan Solihin, and Josep Torrellas. Automatically Mapping Code on an Intelligent Memory Architecture. ***HPCA '01****: Proceedings of the 7th International Symposium on High Performance Computer Architecture*, pp. 121 — 132, Monterrey, Mexico, January 2001, DOI:10.1109/HPCA.2001.903257. (26/110, 23.6%)
53. Yan Solihin, Jaejin Lee, and Josep Torrellas. Adaptively Mapping Code in an Intelligent Memory Architecture. ***IMS '00****: Proceedings of the 2nd Workshop on Intelligent Memory Systems* (in conjunction with ASPLOS-IX, also appears in Springer-Verlag Lecture Notes in Computer Science, Vol. 2107, 2000), pp. 71 — 84, Cambridge, Massachusetts, USA, November 2000, DOI:10.1007/3-540-44570-6_5. (8/29, 27.6%)
54. Jaejin Lee and David A. Padua. Hiding Relaxed Memory Consistency with Compilers. ***PACT '00****: Proceedings of the 2000 International Conference on Parallel Architectures and Compilation Techniques*, pp. 111 — 122, Philadelphia, Pennsylvania, October 2000, DOI:10.1109/PACT.2000.888336. (22/107, 20.6%)
55. Jaejin Lee, David A. Padua, and Samuel P. Midkiff. Basic Compiler Algorithms for Parallel Programs. ***PPoPP '99****: Proceedings of the 7th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming* (also appears in *ACM SIGPLAN Notices*, Vol. 34, No. 8, August 1999), pp. 1 — 12, Atlanta, Georgia, USA, May 1999, DOI:10.1145/329366.301105. (17/79, 21.5%)
56. Jaejin Lee, Samuel P. Midkiff, and David A. Padua. Concurrent Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs. ***LCPC '97****: Proceedings of the 10th International Workshop on Languages and Compilers for Parallel Computing* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 1366, 1998), pp. 114 — 130, Twin Cities, Minnesota, August 1997, DOI:10.1007/BFb0032687.
57. Jaejin Lee and David A. Padua. Parallel Static Single Assignment Form and Constant Propagation for Explicitly Parallel Programs. ***INTERACT-2****: Proceedings of the 2nd Workshop on Interaction between Compilers and Computer Architectures* (in conjunction with *HPCA '97*), San Antonio, Texas, February 1997.
58. William Blume, Rudolf Eigenman, K. Faigin, John Grout, Thomas Lawrence, Jaejin Lee, Jay Hoeflinger, David Padua, Yunheung Paek, Paul Petersen, William Pottenger, Lawrence Rauchwerger, Stephen Weatherford, and Peng Tu. Restructuring Programs for High-Speed Computers with Polaris. *Proceedings of the 1996 Workshop on Challenges for Parallel Processing* (in conjunction with *ICPP '96*), August 1996.
59. Zohar Manna, Nikolaj Bjorner, Anca Browne, Edward Chang, Michael Colon, Luca de Alfaro, Harish Devarajan, Arjun Kapur, Jaejin Lee, Henny Sipma, and Tomas E. Uribe. STeP: The Stanford Temporal Prover. ***TAPSOFT '95****: Theory and Practice of Software Development, 6th International Joint Conference CAAP/FASE* (also appears in *Springer-Verlag Lecture Notes in Computer Science*, Vol. 915, 1995), pp. 793 — 794, May 1995.

PUBLICATIONS (cont'd)

Posters

1. Jungho Park, Hyungmin Cho, Wookeun Jung, and Jaejin Lee. Transparent GPU Memory Management for DNNs, Poster presentation in ***PPoPP '18***: *Proceedings of the 23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 411—412, Vienna, Austria, February 2018, DOI: 10.1145/3178487.3178531
2. Gangwon Jo, Jaehoon Jung, Jiyoung Park, and Jaejin Lee. MAPA: An Automatic Memory Access Pattern Analyzer for GPU Applications, Poster presentation in ***PPoPP '17***: *Proceedings of the 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 443 — 444, Austin, Texas, USA, February 2017, DOI: 10.1145/3018743.3019034
3. Jungwon Kim, Sangmin Seo, Jun Lee, Jeongho Nah, Gangwon Jo, and Jaejin Lee. OpenCL as a Unified Programming Model for Heterogeneous CPU/GPU Clusters, Poster presentation in ***PPoPP '12***: *Proceedings of the 17th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, pp. 299 — 300, New Orleans, Louisiana, USA, February 2012, DOI: 10.1145/2145816.2145863.
4. Jungho Park, Choonki Jang and Jaejin Lee. A Software-Managed Coherent Memory Architecture for Manycores, Poster presentation in ***PACT '11***: *Proceedings of the 20th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 213 — 213, Galveston Island, Texas, USA, October 2011, DOI: 10.1109/PACT.2011.46 (PACT '11 ACM Student Research Competition)
5. Choonki Jang. SRC: An Automatic Code Overlaying Technique for Multicores with Explicitly-Managed Memory Hierarchies, Poster presentation in ***ICS '11***: *Proceedings of the 25th ACM International Conference on Supercomputing*, pp. 377 — 377, Tucson, Arizona, USA, June 2011, DOI: 10.1145/1995896.1995960 (Third place in ICS '11 ACM Student Research Competition)
6. Jun Lee, Sangmin Seo, and Jaejin Lee. A Software-SVM-based Transactional Memory for Multicore Accelerator Architectures with Local Memory, Poster presentation in ***PACT '10***: *Proceedings of the 19th ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques*, pp. 567 — 568, Vienna, Austria, September 2010, DOI: 10.1145/1854273.1854355

Refereed Journal Articles

1. Thanh Tuan Dao and Jaejin Lee. An Auto-tuner for OpenCL Work-group Size on GPUs, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 29, No. 2, pp. 283 — 296, February 2018, DOI: 10.1109/TPDS.2017.2755657
2. Bernhard Egger, Eunbyung Park, Younghyun Jo, Changyeon Jo, and Jaejin Lee. Efficient Checkpointing of Live Virtual Machines, *IEEE Transactions on Computers*, Vol. 65, No. 10, pp. 3041 — 3054, October 2016, DOI: 10.1109/TC.2016.2519890
3. Gangwon Jo, Jeongho Nah, Jun Lee, Jungwon Kim, and Jaejin Lee. Accelerating LINPACK with MPI-OpenCL on Clusters of Multi-GPU Nodes, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 26, No. 7, pp. 1814 — 1825, July 2015, DOI: 10.1109/TPDS.2014.2321742
4. Thanh Tuan Dao, Jungwon Kim, Sangmin Seo, Bernhard Egger, and Jaejin Lee. A Performance Model for GPUs with Caches, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 26, No. 7, pp. 1800 — 1813, July 2015, DOI: 10.1109/TPDS.2014.2333526
5. Choonki Jang, Jaejin Lee, Bernhard Egger, and Soojung Ryu. Automatic Code Overlay Generation and Partially Redundant Code Fetch Elimination, *ACM Transactions on Architecture and Code Optimization*, Vol. 9, No. 2, Article 10, June 2012

PUBLICATIONS (cont'd)

Refereed Journal Articles (cont'd)

6. Seungkyun Kim, Kiwon Kwon, Chihun Kim, Choonki Jang, Jaejin Lee, and Sang Lyul Min. Demand Paging Techniques for Flash Memory Using Compiler Post-pass Optimizations, *ACM Transactions on Embedded Computing Systems*, Vol. 10, No. 4, Article 40, November 2011
7. Bernhard Egger, Seungkyun Kim, Choonki Jang, Jaejin Lee, Sang Lyul Min, and Heonshik Shin. Scratchpad Memory Management Techniques for Code in Embedded Systems without an MMU, *IEEE Transactions on Computers*, Vol. 59, No. 8, pp. 1047 — 1062, August 2010, DOI: 10.1109/TC.2009.188
8. Yoon Jae Seong, Eyee Hyun Nam, Jin Hyuk Yoon, Hongseok Kim, Jin-yong Choi, Sookwan Lee, Young Hyun Bae, Jaejin Lee, Yookun Cho, and Sang Lyul Min. Hydra: A Block-Mapped Parallel Flash Memory Solid State Disk Architecture, *IEEE Transactions on Computers*, Vol. 59, No. 7, pp. 905 — 921, July 2010, DOI: 10.1109/TC.2010.63
9. Jaejin Lee, Jung-Ho Park, Honggyu Kim, Changhee Jung, Daeseob Lim, and SangYong Han. Adaptive Execution Techniques of Parallel Programs for Multiprocessors, *Journal of Parallel and Distributed Computing*, Vol. 70, No. 5, pp. 467 — 480, May 2010, DOI:10.1016/j.jpdc.2009.10.008
10. Jaejin Lee, Changhee Jung, Daeseob Lim, and Yan Solihin. Prefetching with Helper Threads for Loosely-Coupled Multiprocessor Systems. *IEEE Transactions on Parallel and Distributed Systems*, Vol. 20, No. 9, pp. 1309 — 1324, September 2009, DOI:10.1109/TPDS.2008.224
11. Jongsoo Park and Jaejin Lee. A Practical Improvement to the Partial Redundancy Elimination in SSA Form, *Journal of Computing Science and Engineering*, Vol. 2, No. 3, pp. 301 — 320, September 2008, http://jcse.kiise.org/posting/2-3/jcse_2-3_31.pdf
12. Bernhard Egger, Jaejin Lee, Heonshik Shin. Dynamic Scratchpad Memory Management for Code in Portable Systems with an MMU. *ACM Transactions on Embedded Computing Systems*, Vol. 7, No. 2, Article No. 11, February 2008, DOI:10.1145/1331331.1331335
13. Sheayun Lee, Jaejin Lee, Chang Yun Park, Sang Lyul Min. Selective Code Transformation for Dual Instruction Set Processors. *ACM Transactions on Embedded Computing Systems*, Vol. 6, No. 2, Article No. 10, May 2007, DOI:10.1145/1234675.1234677
14. Mazen Kharbutli, Yan Solihin, and Jaejin Lee. Eliminating Conflict Misses Using Prime Number--Based Cache Indexing. *IEEE Transactions on Computers*, Vol. 54, No. 5, pp. 573 — 586, May 2005, DOI:10.1109/TC.2005.79
15. Samuel P. Midkiff, Jaejin Lee, and David A. Padua. A Compiler for Multiple Memory Models. *Concurrency and Computation: Practice and Experience (Special Issue on Compilers for Parallel Computers)*, Vol. 16, No. 2-3, pp. 197 — 220, February-March, 2004, DOI:10.1002/cpe.771
16. Yan Solihin, Jaejin Lee, and Josep Torrellas. Correlation Prefetching with a User Level Memory Thread. *IEEE Transactions on Parallel and Distributed Systems*, Vol. 14, No. 6, pp. 563 — 580, June 2003, DOI:10.1109/TPDS.2003.1206504
17. Yan Solihin, Jaejin Lee, and Josep Torrellas. Automatic Code Mapping on an Intelligent Memory Architecture. *IEEE Transactions on Computers (Special Issue on Advances in High Performance Memory Systems)*, Vol. 50, No. 11, pp. 1248 — 1266, November 2001, DOI:10.1109/12.966498
18. Jaejin Lee and David A. Padua. Hiding Relaxed Memory Consistency with a Compiler. *IEEE Transactions on Computers (Special Issue on Parallel Architectures and Compilation Techniques)*, Vol. 50, No. 8, pp. 824 — 833, August 2001, DOI:10.1109/12.947002
19. Jaejin Lee, Samuel P. Midkiff, and David A. Padua. A Constant Propagation Algorithm for Explicitly Parallel Programs. *International Journal of Parallel Programming*, Vol. 26, No. 5, pp. 563 — 589, October 1998, DOI:10.1023/A:1018772514882

PUBLICATIONS (cont'd)

Refereed Journal Articles (cont'd)

20. William Blume, Ramon Doallo, Rudolf Eigenmann, John Grout, Jay Hoeflinger, Thomas Lawrence, Jaejin Lee, David Padua, Yunheung Paek, Bill Pottenger, Lawrence Rauchwerger, and Peng Tu. Parallel Programming with Polaris, *IEEE Computer*, Vol. 29, No. 12, pp. 78 — 82, December 1996, DOI:10.1109/2.546612

Technical Reports

1. Jaejin Lee and David A. Padua. A Compiler Technique to Hide Relaxed Memory Consistency. Technical Report MSU-CSE-01-13, Department of Computer Science and Engineering, Michigan State University, Michigan, USA, April 2001.
2. Jaejin Lee, David A. Padua, and Samuel P. Midkiff. Basic Compilation Techniques for Explicitly Parallel Programs. Technical Report MSU-CSE-01-14, Department of Computer Science and Engineering, Michigan State University, Michigan, USA, April 2001.
3. Jaejin Lee, Hiding the Java Memory Model with Compilers. Technical Report MSU-CSE-00-29, Department of Computer Science and Engineering, Michigan State University, Michigan, USA, December 2000.
4. Jaejin Lee, Compilation Techniques for Explicitly Parallel Programs. Ph.D. Thesis, Technical Report UIUCDCS-R-99-2112, Department of Computer Science, University of Illinois at Urbana-Champaign, Illinois, USA, October 1999.
5. Jaejin Lee, Samuel P. Midkiff, and David A. Padua. Concurrent Static Single Assignment Form and Concurrent Sparse Conditional Constant Propagation for Explicitly Parallel Programs. Technical Report TR1525, Center for Supercomputing Research and Development, University of Illinois at Urbana-Champaign, Illinois, USA, July 1997.
6. William Blume, Rudolf Eigenman, K. Faigin, John Grout, Thomas Lawrence, Jaejin Lee, Jay Hoeflinger, David Padua, Yunheung Paek, Paul Petersen, William Pottenger, Lawrence Rauchwerger, S. Weatherford, and Peng Tu. Advanced Program Restructuring for High- Performance Computers with Polaris. Technical Report TR1473, Center for Supercomputing Research and Development, University of Illinois at Urbana-Champaign, Illinois, USA, January 1996.

PUBLICATIONS (cont'd)

Patents

1. Jaejin Lee, Jungwon Kim, and Junghyun Kim. Cluster System and Communication Method in Cluster System. **U. S. Patent 10,097,618**, filed January 13, 2015, and issued October 9, 2018.
2. Min-Ju Lee, Bernhard Egger, Jaejin Lee, Young-Lak Kim, Honggyu Kim, and Hongjune Kim. Dynamic Library Profiling Method and Dynamic Library Profiling System. **U. S. Patent 9,959,191**, filed November 22, 2013, and issued May 1, 2018.
3. Min-Ju Lee, Bernhard Egger, Jaejin Lee, Young-Lak Kim, Honggyu Kim, and Hongjune Kim. Dynamic Library Profiling Method and Dynamic Library Profiling System. **Chinese Patent 103838662**, filed November 19, 2013, and issued April 24, 2018.
4. Jaejin Lee and Jungwon Kim. Cluster System Based on Parallel Computing Framework, and Host Node, Computing Node and Method for Executing Application Therein. **U. S. Patent 9,485,303**, filed January 4, 2013, and issued November 1, 2016
5. Jaejin Lee and Jungwon Kim. 2016. Method of Executing Parallel Application on Manycore Cluster System and the Manycore Cluster System. **U. S. Patent 9,396,033**, filed July 1, 2014, and issued July 19, 2016.
6. Jin-Seok Lee, Seong-Gun Kim, Dong-hoon Yoo, Seok-joong Hwang, Jeongho Nah, Jaejin Lee, and Jun Lee. 2016. Apparatus and Method for Generating Vector Code. **U. S. Patent 9,367,291**, filed March 28, 2014, and issued June 14, 2016.
7. Jaejin Lee and Junghyun Kim. 2015. Shared Virtual Memory Management Apparatus for Providing Cache-Coherence. **U. S. Patent 9,208,088**, filed January 1, 2013, and issued December 8, 2015.
8. Seung-Mo Cho, Jong-Deok Choi, and Jaejin Lee. 2015. Method and Apparatus for Transforming Program Code. **U. S. Patent 9,015,683**, filed December 23, 2010, and issued April 21, 2015.
9. Il Hyun Park, Soojung Ryu, Dong-Hoon Yoo, Dong Kwan Suh, Jeongwook Kim, and Choonki Jang. 2015. Processor Including a Cache and a Scratch Pad Memory and Memory Control Method Thereof. **U. S. Patent 9,015,451**, filed March 14, 2008, and issued April 21, 2015.
10. Choonki Jang, Jaejin Lee, Soo-Jung Ryu, Bernhard Egger, Yoon-Jin Kim, Woong Seo, and Young-Chul Cho. 2015. Multiprocessor Using a Shared Virtual Memory and Method of Generating a Translation Table. **U. S. Patent 8,930,672**, filed March 29, 2011, and issued January 6, 2015.
11. Soo-Jung Ryu, Choonki Jang, Jaejin Lee, Bernhard Egger, and Young-Chul Cho. 2015. Apparatus and Method for Generating Code Overlay. **U. S. Patent 8,984,475**, filed March 11, 2011, and issued March 17, 2015.
12. Joo Hwan Lee, Hongjune Kim, Gangwon Jo, Jeongho Nah, Honggyu Kim, Yong-Jun Lee, Jaejin Lee, and Seung-Mo Cho. 2014. Web Browsing Apparatus and Method Through Storing and Optimizing JavaScript® Code. **U. S. Patent 8,887,127**, filed November 22, 2011, and issued November 11, 2014.
13. Jaejin Lee, Jong-Deok Choi, and Seung-Mo Cho. 2014. Unbounded Transactional Memory System and Method. **U. S. Patent 8,706,973**, filed December 9, 2010, and issued April 22, 2014.
14. Jungwon Kim, Jaejin Lee, Kyo-Won Kim, Seung-Kwan Heo. 2013. Method for Scaling Voltage in Mobile Terminal. **U. S. Patent 8,395,701**, filed May 18, 2010, and issued March 12, 2013.
15. Changhee Jung, Dae Seob Lim, Jaejin Lee, Sang Yong Han. 2009. Adaptive Execution Method for Multithreaded Processor-based Parallel System. **U. S. Patent 7,526,637**, filed June 15, 2006, and issued April 28, 2009.

PUBLICATIONS IN KOREAN

Conference and Workshop Papers in Korean

1. 김정욱, 이재진. NUMA 시스템에서 프로그램 로드 위치에 따른 성능 분석, *한국정보과학회 2018 년 한국컴퓨터종합학술대회 논문집*, 1705-1707, 2018 년 6 월, RISS: 105476900
2. 김형모, 이재진. 파스칼 아키텍처 GPU 에서의 스텐실 계산 성능 특성 탐구, *한국정보과학회 2018 년 한국컴퓨터종합학술대회 논문집*, 1643-1645, 2018 년 6 월, RISS: 105476878
3. 박정호, 조강원, 정우근, 김형모, 정재훈, 다오탄뚜안, 박지영, 김정욱, 김희훈, 도영동, 오평석, 이재진. 통합 이종 프로그래밍 환경, *정보과학회지*, 35(10), 18-31, 2017 년 10 월, RISS: 103625426
4. 김희훈, 정우근, 이재진. Multi-GPU 에서 딥 뉴럴 네트워크 학습의 성능 확장성 탐구, *한국정보과학회 2017 년 한국컴퓨터종합학술대회 논문집*, 1474-1476, 2017 년 6 월
5. 박지영, 정재훈, 이재진. FPGA 용 OpenCL 고수준 합성 툴의 성능 이식성, *한국정보과학회 2017 년 한국컴퓨터종합학술대회 논문집*, 85-87, 2017 년 6 월
6. 정재훈, 박정호, 이재진. 쿠다 어플리케이션 바이너리 분석을 통한 지피유 코드 추출 기법, *한국정보과학회 2017 년 한국컴퓨터종합학술대회 논문집*, 46-48, 2017 년 6 월
7. 김정욱, 정우근, 이재진. 다양한 OpenCL 디바이스에서의 OpenCL 2.0 SVM 의 성능 검증, *한국정보과학회 2016 년 한국컴퓨터종합학술대회 논문집*, pp. 1582 — 1584, 2016 년 6 월
8. 신재호, 조강원, 이일구, 이재진. OpenCL 을 이용한 이미지 처리 프로그램의 자동 최적화 방법, *한국정보과학회 2016 년 한국컴퓨터종합학술대회 논문집*, pp. 1494 — 1496, 2016 년 6 월
9. 박지영, 김정욱, 신현일, 이재진. 컴퓨터의 개념 교육을 위한 웹 기반 가상 머신 설계 및 구현, *한국정보과학회 2016 년 한국컴퓨터종합학술대회 논문집*, pp. 1045 — 1047, 2016 년 6 월
10. 정재훈, 조강원, 김정현, 정우근, 이재진. LRC: 고성능 컴퓨팅을 위한 경량 통신 라이브러리, *한국정보과학회 2015 년 한국컴퓨터종합학술대회 논문집*, pp. 33 — 35, 2015 년 6 월
11. 주진영, 김정현, 다오탄뚜안, 이재진. CUDA 와 OpenCL 간 코드변환기 구현을 위한 프로그래밍 모델 차이 분석, *한국정보과학회 2014 년 한국컴퓨터종합학술대회 논문집*, pp. 1615 — 1617, 2014 년 6 월
12. 정재훈, 이재진. OpenCL 개발을 위한 이클립스 기반의 통합개발환경, *한국정보과학회 2014 년 한국컴퓨터종합학술대회 논문집*, pp. 27 — 29, 2014 년 6 월
13. 김홍규, 김홍준, 이강웅, 이재진. ARM 리눅스 환경에서 ltrace 를 이용한 라이브러리 함수 호출 추적, *한국정보과학회 2012 년 한국컴퓨터종합학술대회 논문집*, 39(1A), pp. 140—142, 2012 년 6 월
14. 나정호, 조강원, 강수연, 정우근, 이재진. 컴퓨터의 개념 교육을 위한 가상 머신의 설계 및 구현, *한국정보과학회 2012 년 한국컴퓨터종합학술대회 논문집*, 39(1A), pp. 131 — 133, 2012 년 6 월
15. 나정호, 김홍규, 김홍준, 조강원, 이재진. 자바스크립트 적시 컴파일러를 위한 레지스터 할당기의 구현, *한국정보과학회 2011 년 가을 학술발표논문집*, 38(2A), pp. 194 — 197, 2011 년 11 월
16. 김홍준, 이주환, 조강원, 이재진. 실제 웹어플리케이션 상에서의 자바스크립트 성능 측정에 대한 연구, *한국정보과학회 2011 년 가을 학술발표논문집*, 38(2A), pp. 131 —1 34, 2011 년 11 월
17. 조강원, 김홍준, 이주환, 나정호, 이재진. 자바스크립트 프로그램 최적화를 위한 별칭 분석, *한국정보과학회 2011 년 한국컴퓨터종합학술대회 논문집*, 38(1C), pp. 462 — 465, 2011 년 6 월
18. 이주환, 김정현, 김홍준, 이재진, 최재영, 임선영. SSD 에 대한 리눅스 페이지 캐시의 성능 평가, *한국정보과학회 2010 년 한국컴퓨터종합학술대회 논문집*, 37(1B), pp. 368 — 373, 2010 년 6 월
19. 김홍준, 김정현, 이주환, 이재진, 최재영, 임선영. 사이클 정확도를 반영하는 멀티코어기반 전체 시스템 시뮬레이터, *한국정보과학회 2010 년 한국컴퓨터종합학술대회 논문집*, 37(1A), pp. 283 — 284, 2010 년 6 월

PUBLICATIONS IN KOREAN (cont'd)

Conference and Workshop Papers in Korean (cont'd)

20. 김정현, 서상민, 이재진, 박미경, 이종영, 고태경. 멀티코어 시스템을 위한 캐시 시뮬레이터의 설계와 구현, *한국정보과학회 2009 년 한국컴퓨터종합학술대회 논문집*, 36(1B), pp. 327 — 332, 2009 년 6 월
21. 김승균, 김정원, 이재진. 원격 디버깅을 이용한 명령어 단위 프로파일링 기법, *한국정보과학회 2008 년 종합학술대회 논문집*, 35(1B), pp. 542—546, 2008 년 6 월.
22. 전보성, 이준, 이재진. Cell Broadband Engine 을 위한 소스 대 소스 변환, *한국정보과학회 2008 년 종합학술대회 논문집*, 35(1A), pp. 365 — 366, 2008 년 6 월.
23. 하태준, 서상민, 전보성, 이재진. 임베디드 시스템을 위한 메모리 서브시스템 파라미터의 자동 검출 기법, *한국정보과학회 2008 년 종합학술대회 논문집*, 35(1A), pp. 337 — 338, 2008 년 6 월
24. 김정원, 김승균, 이재진, 정창희, 우덕균. On—Chip SRAM 을 이용한 임베디드 시스템 메모리 계층 최적화, *한국정보과학회 2008 년 종합학술대회 논문집*, 35(1A), pp. 335 — 336, 2008 년 6 월
25. 김지훈, 장춘기, 이재진, 민상렬. Scratch—Pad 메모리를 위한 동적 코드 배치 기법, *한국정보과학회 2005 년 한국컴퓨터종합학술대회 논문집*, (A), pp. 784 — 786, 2005 년 7 월

Journal Articles in Korean

1. 신재호, 조강원, 이일구, 이재진. OpenCL 을 이용한 이미지 처리 프로그램의 자동 최적화 방법, *정보과학회 컴퓨팅의 실제 논문지*, 23(3), 188-193, 2017 년 3 월
2. 정우근, 김정욱, 다오탄뚜안, 박정호, 박지영, 신재호, 정재훈, 조강원, 김희훈, 남형욱, 이재진. 딥 러닝을 위한 HW 시스템 및 SW 라이브러리, *정보과학회지*, 34(9), pp.10 — 20, 2016 년 9 월
3. 조강원, 김정현, 다오탄뚜안, 정우근, 박정호, 이용준, 김홍준, 정재훈, 신재호, 이재진. 슈퍼컴퓨터를 이용한 빅 데이터 분석 중심의 HPC 기술 전망, *정보과학회지*, 34(2), pp. 31 — 42, 2016 년 2 월
4. 김정현, 박정호, 조강원, 다오탄뚜안, 주진영, 정재훈, 김정원, 서상민, 이준, 나정호, 이재진. SnuCL : 이종 매니코어 클러스터를 위한 OpenCL 프로그래밍 환경, *정보과학회지*, 32(5), pp. 66 — 76, 2014 년 5 월
5. 조강원, 서상민, 나정호, 김정원, 김정현, 이준, 박정호, 이용준, 김홍준, 강수연, 주진영, 박선명, 정우근, 임기현, 이재진. 이종 슈퍼컴퓨터 기술 동향과 슈퍼컴퓨터 '천둥'의 개발 사례, *정보과학회지*, 31(4), pp. 34 — 41, 2013 년 4 월
6. 이준, 서상민, 김정원, 조강원, 최완, 이재진. 고성능 컴퓨팅 기술 연구 현황 및 발전 전망, *한국차세대컴퓨팅학회 논문지*, 8(2), pp. 99 — 117, 2012 년 4 월
7. 다오탄뚜안, 김정원, 이재진. 이종 병렬컴퓨팅 환경에서 기계학습을 이용한 접근방법, *정보과학회지*, 29(2), pp. 101 — 109, 2011 년 2 월
8. 박은병, 이용준, 김승균, 이재진, 박경민. 임베디드 환경에서 응용프로그램 시작의 가속 기법, *대한임베디드공학회논문지*, 4(4), pp. 174 — 179, 2009 년 12 월
9. 하태준, 서상민, 전보성, 이재진. 임베디드 시스템을 위한 메모리 서브시스템 파라미터의 자동 검출, *정보과학회논문지 : 컴퓨팅의 실제 및 레터*, 15(5), pp. 350 — 354, 2009 년 5 월
10. 김정원, 김승균, 이재진, 정창희, 우덕균. On-Chip SRAM 을 이용한 임베디드 시스템 메모리 계층 최적화, *정보과학회논문지 : 시스템 및 이론*, 36(2), pp. 102 — 110, 2009 년 4 월
11. 이강웅, 이재진, 신현식. 휴대장치를 위한 응용프로그램 특성에 따른 적응형 전력관리 기법, *정보과학회논문지 : 시스템 및 이론*, 34(7-8), pp. 367 — 376, 2007 년 8 월

PUBLICATIONS IN KOREAN (cont'd)

Journal Articles in Korean (cont'd)

12. 정창희, 이재진. SMT 멀티 프로세서 시스템을 위한 적응형 실행 기법, *정보과학회 프로그래밍언어논문지*, 19(2), pp. 17—32, 2005 년 11 월
13. 이재진. 임베디드 소프트웨어의 Post—Pass 최적화 기법, *전자공학회지*, 31(11), pp. 42 — 48, 2004 년 11 월
14. 이재진. 병렬 프로그램의 적응형 실행 기법, *정보과학회논문지 : 시스템 및 이론*, 31(7-8), pp. 421 — 431, 2004 년 8 월

Korean Patents

1. 이재진, 박정호. 이종 멀티코어 프로세서를 활용한 암호화 처리 장치 및 암호화 처리 방법. Korean Patent 10-1923210(Application No. 10-2017-0007155), filed January 17, 2017, and issued November 28, 2018
2. 이재진, 조강원. 이종 시스템에서의 데이터 분배 기법. Korean Patent 10-1897624 (Application No. 10-2017-0009440), filed January 19, 2017, and issued October 4, 2018
3. 이재진, 조강원, 신재호. 이미지 처리 장치 및 방법. Korean Patent 10-1867423 (Application No. 10-2016-0082233), filed June 30, 2016, and issued June 18, 2018
4. 조승모, 이재진, 이주환, 김홍준, 조강원, 나정호, 김홍규, 이용준. 자바스크립트 코드 저장 및 최적화를 통한 웹 브라우징 방법 및 장치. Korean Patent 10-1782995 (Application No. 10-2011-0003707), filed January 13, 2011, and issued September 22, 2017
5. 이재진, 정우근, 조강원, 김홍준. 분산 처리 시스템 및 분산 처리 시스템에서의 파일 처리 방법. Korean Patent 10-1748210 (Application No. 10-2016-0003923), filed January 12, 2016, and issued June 12, 2017
6. 이재진, 조강원. 프로그램 컴파일 장치 및 프로그램 컴파일 방법. Korean Patent 10-1737785 (Application No. 10-2015-0190701), filed December 31, 2015, and issued May 15, 2017
7. 이재진, 김정원. 클러스터 시스템의 계산 디바이스 가상화 방법 및 그 시스템. Korean Patent 10-1682113 (Application No. 10-2016-0040901), filed April 4, 2016, and issued November 28, 2016
8. 이재진, 장춘기, 류수정, 이강웅, 김윤진, 서웅, 조영처. 공유 가상 메모리를 이용한 멀티 프로세서 및 주소 변환 테이블 생성 방법. Korean Patent 10-1671494 (Application No. 10-2010-0098441), filed October 8, 2010, and issued October 26, 2016
9. 조승모, 최종덕, 이재진. 2016. 무한 트랜잭션 메모리 시스템 및 그 동작 방법. Korean Patent 10-1639672 (Application No. 10-2010-0000614), filed January 5, 2010, and issued July 8, 2016
10. 장춘기, 이재진, 류수정, 이강웅, 조영철. 2016. 코드 오버레이 생성 장치 및 방법. Korean Patent 10-1636521 (Application No. 10-2010-0027515), filed March 26, 2010, and issued June 29, 2016
11. 조승모, 최종덕, 이재진. 2016. 프로그램 코드의 변환 방법. Korean Patent 10-1613971 (Application No. 10-2009-0134367), filed December 30, 2009, and issued April 14, 2016
12. 이재진, 김정원. 2016. 매니코어 클러스터 시스템 상에서 병렬 프로그래밍을 수행하는 방법 및 매니코어 클러스터 시스템. Korean Patent 10-1594915 (Application No. 10-2014-0008392), filed January 23, 2014, and issued February 11, 2016
13. 이재진, 김정원, 김정현. 2016. 클러스터 시스템 및 클러스터 시스템에서의 통신 방법. Korean Patent 10-1592375 (Application No. 10-2014-0187852), filed December 24, 2014, and issued February 1, 2016
14. 이재진, 박정호. 2015. 매니코어 시뮬레이션 시스템 및 방법. Korean Patent 10-1561507 (Application No. 10-2014-0005353), filed January 16, 2014, and issued October 13, 2015

PUBLICATIONS IN KOREAN (cont'd)

Korean Patents (cont'd)

15. 이재진, 서상민. 2015. 워크 그룹 크기 결정 방법, 시스템 및 컴퓨터 판독가능 기록매체. Korean Patent 10-1537725 (Application No. 10-2013-0166372), filed December 30, 2013, and issued July 13, 2015.
16. 이재진, 조강원, 나정호. 2014. 수냉식 클러스터 컴퓨터 냉각시스템. Korean Patent 10-1475376 (Application No. 10-2013-0154127), filed December 11, 2013, and issued December 16, 2014.
17. 김규원, 김정원, 이재진, 허성관. 2014. 휴대단말기의 전압 스케일링 방법. Korean Patent 10-1443399 (Application No. 10-2009-0045130), filed May 22, 2009, and issued September 16, 2014.
18. 이재진, 김정현. 2014. GPU 가상화 시스템. Korean Patent 10-1435772 (Application No. 10-2013-0071605), filed June 21, 2013, and issued August 23, 2014.
19. 이재진, 김정현. 2014. 캐시 일관성 보장을 위한 공유 가상 메모리 관리 장치. Korean Patent 10-1355105 (Application No. 10-2012-0000612), filed January 3, 2012, and issued January 14, 2014.
20. 이재진, 김정원. 2013. 병렬 컴퓨팅 프레임워크 기반의 클러스터 시스템, 호스트 노드, 계산 노드 및 어플리케이션 실행 방법. Korean Patent 10-1332840 (Application No. 10-2012-0001690), filed January 5, 2012, and issued November 19, 2013.
21. 박일현, 류수정, 유동훈, 서동관, 김정욱, 장춘기. 2013. 프로세서 및 메모리 제어 방법. Korean Patent 10-1312281 (Application No. 10-2007-0112852), filed November 6, 2007, and issued September 23, 2013.
22. 이재진, 이준. 2013. 개방형 범용 병렬 컴퓨팅 프레임워크 동적 작업 분배 장치. Korean Patent 10-1284195 (Application No. 10-2012-0002408), filed January 9, 2012, and issued July 3, 2013.
23. 이재진, 장춘기, 박정호. 2012. 멀티코어 시스템 및 멀티코어 시스템의 메모리 관리 장치. Korean Patent 10-1192423 (Application No. 10-2010-0134895), filed December 24, 2010, and issued October 11, 2012.
24. 이재진, 김정원. 2012. 개방형 범용 병렬 컴퓨팅 프레임워크(OpenCL)에서의 메모리 접근영역 분석장치 및 그 방법. Korean Patent 10-1157596 (Application No. 10-2010-0134898), filed December 24, 2010, and issued June 12, 2012.
25. 이재진, 장춘기, 박정호. 2012. 멀티코어 시스템의 메모리 관리 장치 및 방법. Korean Patent 10-1155127 (Application No. 10-2010-0134896), filed December 24, 2010, and issued June 4, 2012.